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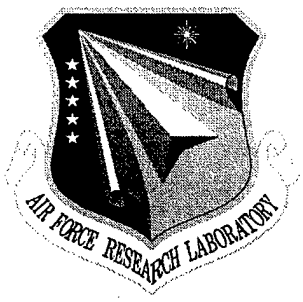

DEVELOPMENT AND APPLICATION OF JOSEPHSON EFFECT SUBMILLIMETER WAVE SOURCES

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DEVELOPMENT AND APPLICATION OF JOSEPHSON EFFECT SUBMILLIMETER WAVE SOURCES

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Sergey Tolpygo

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13. ABSTRACT *(Maximum 200 words)*
Submillimeter wave oscillators with power approaching 0.5 mW were developed based on distributed arrays of wide Josephson junctions. The report describes the achievements in design fabrication technology, methods of coupling the oscillator power off-chip and spectral measurements as well as the possible limitations on the oscillators power related to the device physics. It is shown that distributed arrays of wide self-shunted junctions are promising for the future development of submillimeter wave sources with more than 1 mW power.

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1. Project goals

The goals of this project were to develop the technologies and understanding needed for high-power submillimeter wave sources based on arrays of Josephson junctions. As a demonstration, it was planned to build a submillimeter wave source with power levels in the mW region. It was also planned to make a self contained portable source where the oscillator power could be coupled off chip and out of the cryostat. As a one of the possible applications, it was proposed to demonstrate the operation of an integrated SIS receiver using a Josephson array source for its LO. Achieving these goals required considerable advances in fabrication technology, device physics, design concept, and instrumentation. This report describes our main achievements in these key areas as well as the results on planned demonstrations such as higher power Josephson-junction-array wave sources, coupling the radiation off chip and out of the cryostat, and an SIS receiver for off chip power and linewidth measurements.

2. Background

During the previous contracts [1]-[2], submillimeter wave sources based on the Josephson effect had been developed to a point where it was feasible to demonstrate some small system applications using these sources. Three major results had been obtained.

1. The operation of series biased arrays of 100 junctions had been demonstrated. In all previous arrays the junctions were biased in parallel in order to compensate for the uniformity in the junction parameters.

2. A much more compact design of the distributed arrays had been demonstrated. In the initial distributed arrays, the junctions were placed at intervals of one wavelength. This resulted in a very long microstrip which both contributes a significant power loss and takes a large area on the chip. In the new design, approximately 50% of the length of the microstrip can be occupied by junctions placed at locations where stable phase locking should occur.

3. We had measured the linewidth of the radiation from a distributed 10-junction array near the submillimeter wave range. The measured linewidth agreed well with theory and extrapolated to 100 kHz for a 100-junction array, giving evidence that the required linewidths can be achieved at $N > 100$, where N is the number of junctions in the array.

3. Results

3.1. Demonstration and development of higher power array oscillators

It is known that arrays capable of delivering milliwatts of power should contain thousands of coherently oscillating Josephson junctions. Since the critical current of each junction can reach tens of milliamps, the parallel biasing scheme is clearly impractical because the total bias current would be N times the bias current of a single junction (N is the number of junctions in the array), which can easily reach tens of amps. Therefore, an important advance was the demonstration that successful operation can be achieved in large arrays in which the junctions are biased in series [3,4]. Distributed arrays of 500 resistively shunted junctions were designed, fabricated and tested. The 6-μm^2-junctions were placed in groups of ten junctions, 10 μm apart. Adjacent groups were separated by one wavelength at the designed frequency of 390 GHz. The junctions in the array were biased in series using a common dc current. Testing of this array showed complete phase locking of all the junctions in the array. The maximum measured rf power coupled to a 68 Ω load at 394 GHz was 47 μW and 10 μW at 500 GHz. This work is described in detail in Appendix A.

Since the rf power is proportional to I_c^2, where I_c is the critical current of the junction, a further increase in power can be achieved by increasing both the junction critical current density j_c and the junction area. However, there are certain restrictions and limitations on this approach, which needed to be worked out. Firstly, the junction length (in the direction of the bias current) should be kept smaller than the Josephson penetration depth λ_J in order to avoid vortex instabilities in the junction, i.e. only the junction width, w, is allowed to be increased. Moreover, as j_c increases, the junction length should actually decrease since λ_J decreases, being inversely proportional to the square root of the critical current density. Therefore, the critical current of the junction becomes proportional to $j_c \lambda_J w \sim j_c^{1/2}$, and hence the maximum power grows as $j_c w^2$.

Another principle consideration is whether there are possible limitations on the width of the junctions due to, e.g., flux flow instabilities or internal resonances which can develop in wide junctions (of course the bias current should be fed uniformly into wide junctions). To study this, junctions of various widths were incorporated in microstrip resonators designed to operate at 400 GHz, the planned operating frequency of the array. By measuring the self-induced step in the I-V curve of the junction due to the resonance, it was possible to determine the rf current being delivered to the resonator by the junction. By comparing this with that expected from a point junction, internal instabilities in the junction could be detected. The results of these tests proved that junctions up to 160 μm wide show no instabilities. This width was about $15\lambda_J$ and nearly 1/2 the wavelength in the transmission line.

Based on these results, higher oscillator power distributed series arrays of wide junctions were designed and fabricated [5]. One of these arrays contained 250 resistively shunted junctions of 160 μm width. Another array contained 494 junction of 80 μm width. The junctions were clustered in groups of six. Junction groups were separated by half wavelength at the 400 GHz

operating frequency. The junction length was 2 μm. The critical current density was 6 kA/cm^2, which gave λ_J = 5 μm and I_c = 20 mA, and 10 mA for the first and second designs, respectively. These arrays delivered, respectively, an estimated rf power of 0.3 mW and 0.4 mW at 400 GHz to on-chip 8 Ω loads. At 500 GHz the power delivered by the second array was 0.25 mW. The power measurements were done using video mode detection, i.e. by measuring suppression of the critical current of the detector junction. Both the power and the frequency of these sources were roughly twice that of the best results reported before (these results were reported by NIST for large one dimensional arrays that basically copied our earlier designs [3] but used wider junctions). The spectral power measurements showed that the arrays liked to operate in certain relatively narrow frequency bands. The main peak in power occurred at the designed operating frequency of 400 GHz but power was also available at many other frequencies [5]. For instance, strong peaks in the rf power occurred at around 250 GHz and around 500 GHz, which corresponds to the plasma frequency of the junctions in the array and its second harmonics. Other observed peaks could also be due to the existence of other internal resonances, e.g., associated with the shunt resistor loops.

These findings forced us to look deeper into other possible limitations on the array power, which could be related to the device physics or existing junction design. One of these stems from the requirement of multioctave tunability of the wave source. In order to have stable array operation and also to possess this tunability, the junctions in the array should be nonhysteretic, i.e. overdamped, which was usually achieved by shunting intrinsically hysteretic (underdamped) tunnel junctions by external resistors. Apart from an obvious Joule heating, these shunt resistors, unfortunately, create additional inductive loops with the typical inductance $L_s \geq$ 0.2 pH-μm, set by the fabrication limits. Extensive computer simulations performed under this contract have shown that, for a nonchaotic and nonhysteretic array operation, L_s must be less than L_J, where $L_J = \Phi_0/2\pi I_c$ is the Josephson inductance. This limits I_c from above, requiring it to be less than 0.16 mA per micron of the junction width. On the other hand, the plasma frequency of the junction $f_p = (j_c/\Phi_0 C_s)^{1/2}$, where C_s is the specific junction capacitance, should be higher than the operation frequency, f_{op}. For a given operation frequency this limits the critical current density of the junctions from below. For instance, at f_{op} = 1 THz the j_c must be higher than 0.2 mA/μm^2 (20 kA/cm^2). Being combined with the upper limit on the linear current density set by the shunt inductance, $J_c \leq 0.16$ mA/μm, this requires that the maximum length of the junctions be less than 1 μm, that is a submicron fabrication.

3.2. Development of the fabrication technology and submicron junctions with high critical current densities

As it follows from the above, fabrication of high power Josephson junction arrays requires the ability to fabricate highly uniform, submicron-size junctions with high critical current densities. Therefore, an important part of the work was devoted to the development of our planarized photolithographic process, our non-planarized EBL process, and finally our planarized EBL process. Most important results of this work [6]-[8] are described in Appendix

B. One of the major advances here was the successful fabrication of the Josephson junctions which are intrinsically nonhysteretic and thus do not require any external shunts [8]. This was achieved by going to very high critical current densities of over 1 mA/μm^2 (10^5 A/cm^2). At such high values of j_c, the subgap resistance becomes essentially equal to the normal resistance of the junction, in contrast to low-j_c hysteretic junctions where the subgap resistance is much higher than the R_n. Implementation of these self-shunted junctions in array oscillators would eliminate most of the problems discussed above and caused by shunt resistors. The major difficulty in this work – aside from learning how to grow the high-j_c trilayers and achieve necessary junction uniformity – is that the junctions must have deep submicron dimensions in order to reduce heating and self-field effects. To obtain the information necessary for the array design with these high-j_c junctions, phase locking was studied in two-junction cells of different inductance. The cells had junctions ranging in length from 0.25 μm to 1 μm and width from 5 μm to 20 μm. A number of chips with 16 cells per chip were fabricated using 30 kA/cm^2 and 250 kA/cm^2 trilayers. In both cases, a stronger phase locking was found in the shortest junctions. Overall, phase locking was observed from about 300 GHz to 1.4 THz with the locking strength from about 50% of I_c at lower frequencies to about 20% of I_c at the gap frequency. These results showed that high-j_c junctions are indeed very promising for high power submillimeter array oscillators. Phase locking results in high-j_c junctions were reported at Applied Superconductivity Conference (ASC'98) in Palm Desert, California and will be submitted for publication.

3.3. Development of a portable source and off-chip measurements

Another part of the effort was focused on the development of methods of coupling the array radiation off chip and on off-chip measurements of power and radiation linewidth [9],[10]. Along with the high-power array described above, several lower power oscillators coupled to a 75 Ω spiral antenna to radiate power off chip were designed and fabricated. The array used had 300 relatively narrow junctions (width 18 μm) and therefore had much lower available power (about 10 μW) than the 0.4 mW measured from the wide junction arrays described above. The spiral antenna was mounted on a Si hyperhemispherical lens with antireflection coating. The radiation power was detected using an off chip silicon composite bolometer mounted at the apex of a Winston cone in the same cryostat [9]. While the maximum power detected was 0.5 μW at 270 GHz, much smaller than the array can generate, it nevertheless exceeded all previously published values for Josephson radiation coupled off-chip. In further experiments, the radiation power was coupled into free space, out of the dewar, and into another dewar where it was detected by the bolometer [10]. The next advance in this work was the replacement of the bolometer detector with a SIS mixer. This allowed us to obtain both the spectral information and power from the array sources. The SIS mixer consisted of two Josephson junctions in series which were integrated with the hybrid antenna (an on-chip spiral antenna + hyperhemispherical lens) mounted in a separate dewar. The spectrum of power from the array source was observed using second or third harmonic mixing with 88 GHz Gunn generator as a local oscillator. Intermediate frequencies of up to 18 GHz were used, permitting coverage of a significant part of the emitted spectrum [11]. This part of the work is described in more detail in Appendix C.

Interesting results were obtained on injection locking of arrays to narrow their linewidth. These measurements were performed on a small (21 junction) array microwave source operating at about 16 GHz so that it was easy to couple radiation off-chip and measure the spectrum. The natural linewidth of this phase locked array was about 2 MHz, and the output power was about 1 nW. By injecting less than 10 pW power (i.e. a power of less than 1% of the array's power) from a high stability source, it was possible to narrow the linewidth of the array to that of the source–in this case 10 Hz! Thus, a linewidth reduction of over 10^5 was achieved without any loss in output power. Successful locking was also achieved using injection of subharmonics of the array frequency, down to the 4^{th}.

A part of the work was devoted to studying the possibility of creating a millimeter wave maser based on the fluxoid transitions in SQUIDs. It was found that it is possible to pump the SQUID to excited levels within a fluxoid state by using 100 GHz photons when the photon energy equals the level spacing. In this respect, the SQUID is like an artificial "atom" in which the level spacing and the lifetime of the excited states can be controlled. Theoretical analysis done in the mid-eighties predicts that stimulated emission of radiation between fluxoid states should be possible. One of the key requirements for the operation of such a maser is that a population inversion must be achieved. This population inversion (sometimes referred to as a negative temperature) was successfully demonstrated in our work published in Physical Review Letters [12]. It was shown that the system spends 92% of the time in the higher energy state when pumped by weak 100 GHz radiation. This is to be contrasted with the expected thermal population of 1×10^{-20} of the excited level. More details of this work can be found in the review article [13].

4. Summary

A technology for fabricating large arrays of Josephson junctions with submicron dimensions and high critical current densities on 2" Si wafers has been developed. Millimeter and submillimeter wave sources based on series arrays of Josephson junctions capable of delivering up to 0.5 mW of power to on chip loads have been demonstrated. Coupling of array radiation off chip and out of the cryostat by quasioptical techniques as well as using a SIS receiver for off chip power and spectral measurements have been demonstrated. Limitations on the maximum array power and methods of narrowing the radiation linewidth have been studied.

Two Ph.D. theses resulted from work under this contract: "Development of high power submillimeter Josephson array oscillator" by Wenxing Zhang in 1996 and "Macroscopic quantum phenomena in an rf SQUID" by Richard P. Rouse in 1996. A third thesis one "High-power Josephson array oscillators for terahertz frequencies" by Steffen Deus is under preparation and expected to be presented by the end of 1998.

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Appendix A

Demonstration of Josephson effect submillimeter wave sources with increased power

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A submillimeter wave source based on a new design using Josephson junction arrays has been developed and tested. The maximum rf power, delivered to a 68Ω load and detected on chip, was 47 μW at 394 GHz. Significant power was detected at a number of frequencies from 300 to 500 GHz where the power was 10 μW. The observed power at the designed operating frequency near 400 GHz is consistent with all 500 junctions in the series biased array delivering current in phase to the loads. This is in agreement with simulations of smaller arrays of the same design. The linewidth, inferred from the measured resistance at the point of maximum power, with $T=4.2$ K, is less than 1 MHz. The minimum inferred linewidth near 400 GHz, at somewhat lower power, is about 100 kHz.

Many submillimeter wave (SMW) frequency applications, such as radio astronomy and high speed communication, require a compact SMW source capable of delivering rf power in the range of 10–100 μW. For frequencies above 300 GHz, the lack of compact sources is particularly serious requiring increasingly inefficient multiplication of millimeter wave sources. Lately there has been a substantial effort to develop Josephson effect sources, which can work to at least 1 THz,[1] for applications in the SMW.[2–4] The most promising results, recently obtained, have come from three types of sources: long single junctions flux flow oscillators,[2] various types of two-dimensional arrays of small junctions,[3] and one-dimensional (1D) small junction arrays,[4] discussed here. In general a power of about 1 μW is obtained from these sources, although in many cases the source impedance is less than 1 Ω. The highest rf power previously reported from a Josephson effect oscillator has been 7 μW at ~300 GHz by Wan *et al.*[4] using a 1D array. Here we report results from an improved design for Josephson SMW sources—distributed linear arrays of 500 Josephson junctions with series dc biasing—generating an rf power of 47 μW around 394 GHz and 10 μW at 500 GHz into an on-chip load of 68 Ω.

Small resistively shunted junctions (RSJ), described by the RSJ model,[5] are characterized by a critical current I_c and a shunt resistance R_J, and generate a peak rf voltage $V_{rf}=\gamma V_c$ ($V_c \equiv I_c R_J$) with a source impedance Z_s at the Josephson frequency, $f_J=483.6$ GHz/mV. For bias voltage $V>V_c$, $\gamma \to 1$, and $Z_s \to R_J$. The junctions are placed in a superconducting microstrip and interact via the rf current, I_{rf} generated in the microstrip by the Josephson oscillations. For properly designed arrays[6] the rf voltages across the junctions can be made to add in series. This will be true independent of the relative polarities, along the microstrip, of the junctions' biases, i.e., the dc voltage can sum to NV_c (series bias) or to zero (parallel bias). The power from such an array (see Fig. 1) is then just

$$P_N = \kappa \frac{(\gamma N V_c)^2 R_L}{2(NR_J+R_L)^2}. \quad (1)$$

Here N is the number of rf series elements in the array, and R_L is the load impedance seen by the array. $\kappa=1$ is the ideal case, but is in general somewhat less than unity due to losses in the coupling structure or imperfect phase alignment of the junctions. For 1D arrays [Figs. 1(a)–1(c)], N is just the number of junctions in the array. For 2D arrays [Fig. 1(d)] of the types so far reported, the rf current flow is ideally along rows of junctions, with the phase of the rf current transverse to this flow (i.e., across a column) being constant. Equation (1) can then be applied to 2D arrays as well if one replaces N by N_s, the number of series elements (i.e., columns) in the array and R_J by R_{J_s} the resistance of a series element. The power from an array matched to the load, i.e., with $N_s R_{J_s}=R_L$, is $P_N=(N_s V_c)^2/8R_L$, and can in principle be increased just by increasing N_s while keeping NR_J and V_c constant. This implies that $I_{cs} \propto N_s$ and $P_N=R_L I_{cs}^2/8$.

Increasing the source power, therefore, requires increasing I_{cs}, adding together enough series elements to match the array impedance to the load and maintaining phase coherence throughout the array. In practice, there are two essential limitations to this increase. First, when I_{cs} becomes greater than several milliamps, there exists the potential for flux flow instabilities which would dissipate power internally in both single junctions and in the columns of 2D arrays. It is not yet clear whether there is an advantage to 1D or 2D arrays for maximizing I_{cs} while maintaining phase stability. The second problem, common to both 1D and 2D arrays, is that when the length of the array becomes an appreciable fraction of the wavelength, care must be taken to maintain the proper phase relationship between the junction oscillations and the rf current throughout the array. This is required so that all junctions phase lock in a stable manner and provide current to the load with the same phase. Especially for the SMW source, this problem must be solved to permit the use of enough junctions to obtain power levels much above a microwatt. It is this second problem which we address in this paper.

Fully coherent 1D arrays have been demonstrated using both a lumped circuit design[6] [Fig. 1(a)], where the array length $L<\lambda/10$ (λ is the wavelength in the microstrip coupling the junctions), or the so-called quasilumped design where the junctions' spacing is λ.[4] The number of junctions

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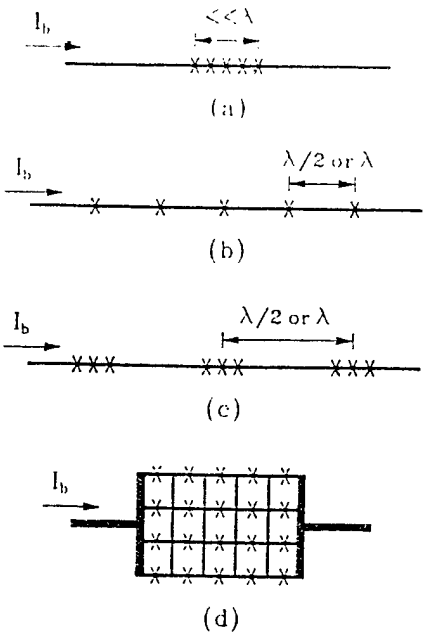

FIG. 1. Some typical structures for Josephson junction arrays: (a) 1D lumped array, (b) quasilumped array, (c) distributed array, and (d) 2D array. λ is the wavelength at the primary operating frequency; I_b is the dc bias current.

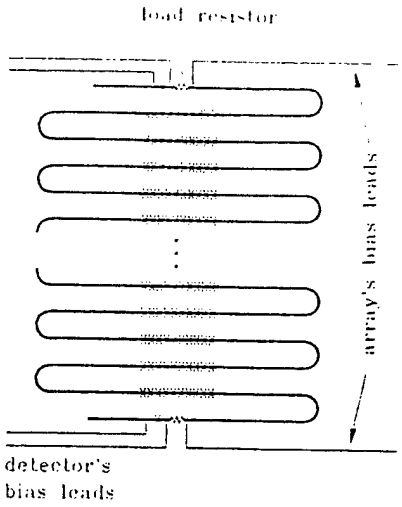

FIG. 2. Schematics of the $N=500$, $M=10$ serial biased 1D distributed Josephson junction array for SMW generation.

in both designs is severely limited in the SMW. A maximum of about $N=10$ can be used in the SMW for lumped arrays made with standard fabrication technologies. For quasilumped arrays, losses in the microstrip coupling the junctions as well as the larger array size are limitations. Much denser packing can be achieved if the junctions can be distributed along the microstrip for a significant fraction of λ. Figure 1(c) shows such a structure where groups of M junctions are placed at intervals of λ or $\lambda/2$ along the microstrip. Our computer simulation shows that for same N and M arrays with $\lambda/2$ interlump distance has a wider tuning range.

Distributed arrays (shown in Fig. 2) of 500 junctions have been designed, fabricated, and tested for SMW generation. Resistively shunted $Nb/AlO_x/Nb$ tunnel junctions are placed in groups of ten junctions ($M=10$) with adjacent junctions in the group separated by 10 μm. Adjacent groups are separated by one wavelength at the designed primary operating frequency of ~390 GHz. Load resistors and Josephson junction detectors to measure the rf currents are placed at both ends of the array. The arrays were fabricated at IBM using planarized all-refractory technology for superconductivity[7] with high critical current density ($J_c \approx 40-60$ kA/cm^2) $Nb/AlO_x/Nb$ trilayers made at AT&T Bell Laboratory. 700 nm of thermally evaporated SiO was used as the dielectric between the Nb microstrip and the 300 nm Nb ground plane, which was placed on top of the array. Each load resistor and detector junction has independent dc bias leads allowing their parameters to be determined using four terminal measurements. R_J is measured by suppressing the junctions' critical current with a magnetic field. The capacitance of the 6 μm^2 junctions, including parasitic capacitance, is estimated from the geometry and the specific capacitance of 46 fF/μm^2 to be ~290 fF. The parasitic inductance L associated with the external shunt resistor is 0.18 pH estimated from the physical dimensions of the shunt. The junctions in the array are biased in series using a common dc current. This requires a higher degree of junction uniformity, but is important for larger arrays. For example, the arrays studied here would have required a bias current of over 2 A for parallel bias instead of the 5 mA actually used.

The coherent rf current generated by the array is measured by the detector junctions placed after the lumped resistor loads. The magnitude of the $n=1$ Shapiro step[8] is used to obtain the amplitude of the coherent rf current I_{rf} through the detector junction and the load resistor by fitting the measured IV curve to that of numerical simulations using measured junction parameters. For numerical simulations, the detector junction has to be described by the resistively inductively and capacitively shunted junction model[9] due to the rather large value of LI_c.

Five samples have been completed and tested for SMW generation. All delivered more than 20 μW of rf power near 394 GHz to loads of about 65 Ω. For the sample W11D8, the average critical current of the junctions in the array is $I_c=3.2$ mA and the average junction resistance is $R_J=0.38$ Ω. The detector junctions have an $I_c \approx 3.5$ mA, and a $R_J=0.38$ Ω. The maximum power from the array occurs at 394 GHz; however, significant power is available at a number of frequencies in the 300–500 GHz range with 10 μW of power delivered to the loads at 500 GHz. Figure 3 shows the measured IV curve of a detector around the $n=1$ Shapiro step with the array operating at 394 GHz and $T=1.9$ K. This is compared with that of the detector simulation using the measured junction parameters and a rf current amplitude from the array of $I_{rf}=1.18$ mA. The measured total load resistance is 68 Ω for this sample giving a rf power, $I_{rf}^2 R_L/2 \approx 47$ μW at

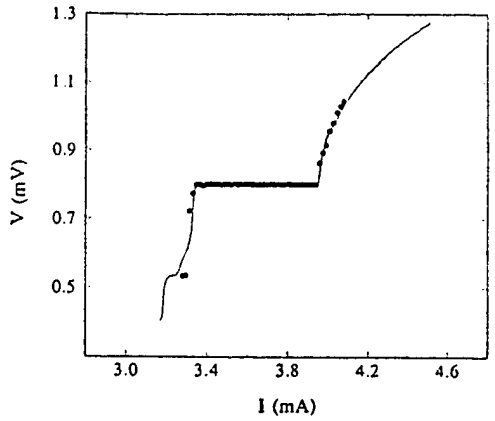

FIG. 3. The measured IV curve (solid line) around the $n=1$ Shapiro step at 798 μV of the detector junction on the sample W11D8 under 394 GHz irradiation from the array and the IV curve obtained from computer simulation (solid circles) using the RICSJ model. The parameters used for the stimulation are $I_c=3.47$ mA, $C=294$ fF, $L=0.178$ pH, $R_J=0.377$ Ω, and $I_{rf}=1.18$ mA. This rf current amplitude corresponds to a power of 47 μW in the load of 68 Ω.

394 GHz. Since the total array resistance is 190 Ω (the actual junctions shunt resistors were somewhat greater than the design values) the maximum available power from this array (into a 190 Ω load) would be 64 μW at 394 GHz.

The measured power of ~50 μW at 394 GHz compares reasonably with the value of 96 μW from Eq. (1), assuming perfect alignment of the junctions' phases and no transmission line losses (i.e., $\kappa=1$). However, κ is in general always less than unity due to imperfect phase alignment and the losses in the coupling structure (in our case, a microstrip transmission line). The measured value of $\kappa=47/96=0.49$ at 394 GHz can be entirely accounted for by a surface resistance of 7 mΩ, assuming nearly perfect phase alignment. Our computer simulations of an array with $N=100$ but otherwise identical in structure to that measured indeed show a negligible phase spread among the junctions. Although the surface resistance of the actual sample has not been measured, the value inferred from the rf power measurement (7 mΩ) is consistent with the measured surface resistance at about 400 GHz in Nb/SiO/Nb microstrip resonators[10] and compares favorably to that obtained by Cucolo *et al.*[11]

The second major advantage of the phase-locked array source is that the radiation linewidth can be substantially reduced since the phase locking suppresses the frequency modulation of the array due to the random noise sources associated with the junction shunt resistors. The linewidth of a series array of N identical Josephson junctions is approximately given by[6,12,13]

$$\Delta f \simeq \left(\frac{2\pi}{\Phi_0}\right)^2 \left(\frac{k_B T}{\pi R_J}\right) \frac{R_d^2}{N} [1+2\alpha^2 x \coth(x)],$$

$$x \equiv \frac{hf}{2k_B T}, \qquad (2)$$

where k_B is Boltzmann's constant, h is Planck's constant, Φ_0 is the magnetic flux quantum, R_d is the dynamic resistance of an independent junction, and $\alpha=0.42$ is the down conversion coefficient. Equation (2) requires some modification in distributed arrays, since the strength of the locking can depend on the position of the junction. However, direct measurements of the linewidth[13] in a small array consisting of two groups of junctions separated by $\lambda/2$ show that, within a factor of 2–3, Eq. (2) provides a reliable estimate of Δf. Using values of R_d and R_J as the average over the array, the implied linewidth at 394 GHz is about 730 kHz at $T=4.2$ K decreasing to 475 kHz at 1.6 K, where $x=5.9$, so zero point fluctuations dominate. The value of R_d varies with bias current giving a minimum implied linewidth of about 100 kHz at $T=4.2$ K near 375 GHz but with a somewhat lower power level.

In summary, 500 junction Josephson effect arrays using dc series bias and a distributed junction layout have been designed, fabricated, and tested. The measured maximum coherent rf power coupled to a 68 Ω load at 394 GHz is 47 μW, implying an available power of 64 μW. A rf power of 10 μW has also been measured at 500 GHz from the array oscillator. At 4.2 K the linewidth near 400 GHz, calculated from Eq. (2) using the measured array parameters, is less than 730 kHz.

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Development of Josephson Oscillators as Millimeter and Submillimeter Wave Sources

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Abstract—Significant progress has been made in recent years on the development of compact millimeter and submillimeter wave sources based on Josephson effect oscillators. Properties of major types of practical Josephson oscillator are reviewed and the most recent result of one-dimensional array oscillator is presented.

I. Introduction

In recent years much progress has been made in the development of compact millimeter (mm) and submillimeter (sub-mm) wave source based on various Josephson oscillators (JO). Josephson oscillators have been demonstrated to produce maximum power of several tens of microwatt in the sub-mm range coupled to usable load [1]. Direct linewidth measurements of various JO yield results in good agreement with the theory [2]–[5]. Relative linewidths of $\Delta f/f \leq 10^{-6}-10^{-5}$ have been achieved. The operating frequency of JO has been shown to extend from less than 100 GHz to about 650 GHz (with power level above 1 μW). Effort in making sub-mm integrated receiver using Josephson local oscillator and SIS mixer has shown a very promising result [4]. These developments lead us to believe that JO has a strong potential in applications such as airborne or spaceborne radioastronomy and satellite communication. For these applications in addition to the common requirement of adequate output power level, narrow linewidth, and wide tuning range, the compactness and low power consumption also play an important role in the selection of the suitable sources. In this article we discuss the mechanism, design principle, and experimental results of three primary types of JO (with emphasis on the one-dimensional Josephson array oscillators) and analyze the major remaining problems and the possible solutions in developing JO into practical mm and sub-mm wave sources.

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II. Josephson Oscillators

A Josephson oscillator is a device based on the famous ac Josephson effect: a Josephson junction generates microwave at frequency $f = V/\Phi_0$, where V and Φ_0 are the average voltage across the junction and the magnetic flux quantum, respectively. This relation gives $f/V = 483.6$ GHz/mV which means that a Josephson junction is a linear voltage controlled oscillator and is a promising source for mm and sub-mm wave (*i.e.* V from a few hundred μV to a few mV).

However, there are several problems, such as low output power, wide linewidth, and low source impedance, associated with the single junction source. These problems can be solved by phase-locking N Josephson junctions in an array to produce coherent in-phase oscillations. For instance, when completely phase-locked, the power coupled to a *matched* load from an array of N identical junctions increases as N^2 while the linewidth decreases as $1/N^2$. In addition, source impedance of the array can be readily matched to that of the load. In this paper we make a brief analysis of the advantages and disadvantages of several types of Josephson effect oscillator with emphasis on the design concept, fabrication technology, and experimental results of 1D Josephson junction sub-mm source.

A. Single small junction

The simplest JO is a small Josephson junction whose dimension is much smaller than the Josephson penetration depth λ_J. It is easy to design and produce with the present day fabrication technology. Although it has good frequency tuning range, single junction source suffers from low output power, wide linewidth, and low source impedance. For instance, the maximum rf power that can be extracted from a resistively shunted Josephson junction (RSJ) having critical current I_c and shunt resistance R_J to a *matched* load R_L is approximately given by

$$P_1 \simeq \frac{(\kappa V_c)^2}{8R_L}, \tag{1}$$

where κ depends on junction's bias current and is usually less than unity. Hence, P_1 is less than a few μW due to the fundamental constrain of $I_cR \leq 3$ mV for junctions available at the present time. Assuming the low

frequency noise current flowing through the junction is dominated by the Johnson noise of the shunt resistor (neglect the noise down-converted from that of at Josephson frequency) the radiation linewidth of a single junction is then given by

$$\Delta f_1 = \frac{4\pi}{\Phi_0^2}\frac{R_d^2}{R_J}k_B T, \tag{2}$$

where R_d is the dynamic resistance of the junction at voltage $V = f\Phi_0$. For a junction of $R_J = 1\ \Omega$ operating at 4.2 K the linewidth is greater than 160 MHz (assuming $R_d = R_J$), which is unacceptable for most application.

B. Flux flow oscillator

The second type of single junction oscillator is the flux flow oscillator (FFO) which is a long Josephson junction operated in the viscous unidirectional flux-flow regime. A typical FFO can be formed by a junction having $w \ll \lambda_J \ll L$, where w and L are the width and length of the junction. When in operation, fluxons are created at one end of the junction by applying a magnetic field and are driven to the other end by the Lorentz force between the fluxons and the biasing current. The oscillation frequency of a FFO is given by $f = V/\Phi_0 = nuL$, where n is the number of fluxons in the junction and u is the average phase velocity of the flux-flow. FFO can be tuned over a fairly wide frequency range by changing magnetic field and/or bias current. The early investigations of FFO by Nagatsuma *et al.*[6] shown very promising results. Recently, it was demonstrated that an FFO is able to couple maximum power of $\sim 1\ \mu$W to an SIS mixer of 45 Ω [3], [4]. The radiation linewidth of an FFO is also given by Eq. 2. Relative linewidth $\Delta f/f$ in the range of 10^{-5} to 2×10^{-6} has been obtained by several groups [3], [4], [7]. FFOs have proven to generate more power and narrower linewidth than single small junctions without sacrificing too much frequency tuning range. However, this is achieved by adding magnetic field as an extra control parameter which not only increases the complexity of operation but also makes it unsuitable for applications where rapid tuning of local oscillator's frequency is required. Although the output power of a FFO is adequate for a SIS mixer it is still too low for off-chip application for which more than tens of μW power are needed. The problem of low source impedance still exists for FFO. It can be circumvented by using impedance matching transformer at the expense of reducing the frequency tuning range.

C. One-dimensional array

The use of one-dimensional (1D) series array of N identical junctions as mm and sub-mm wave source was proposed more than 20 years ago [8]. Some typical 1D array structures are shown in Fig. 1(a)-(c). If all junctions oscillate in-phase, the power that can be extracted to a load R_L from such an array is

$$P_N \simeq \frac{(\kappa N V_c)^2 R_L}{2(NR_J + R_L)^2}. \tag{3}$$

In the case of a *matched* load $R_L = NR_J$, Eq. 3 is reduced to

$$P_N \simeq \frac{N^2 V_c^2}{8R_L} = N^2 P_1.$$

Hence, the power produced by a 1D array is N^2 times that of a single junction. On the other hand, since noises generated from junction resistors add incoherently while signals produced at Josephson frequency by junctions add coherently, the radiation linewidth of a 1D array can be greatly reduced from that of a single junction and is given by:

$$\Delta f_N = \frac{4\pi}{\Phi_0^2}\frac{R_d^2}{N^2 R_J}k_B T = \frac{\Delta f_1}{N^2}, \tag{4}$$

where R_d and R_J is the dynamic and shunt resistance of the unperturbed junction. The problem of impedance matching can be solved easily by choosing an appropriate number of junctions in the array such that $NR_J = R_L$. It should be pointed out that Eq. 3 can be rewritten as $P_N = I_c^2 R_L/8$ which sets a limit on the maximum power that can be extracted from a 1D array to about 0.6 mW (assuming a critical current of 10 mA and a load of 50 Ω). Higher power can be obtained for load impedance greater than 50 Ω.

It is very important to note that the advantages of a 1D array discussed above depends on the complete in-phase oscillation (mutual phase-locking) of all N junctions. In practice, it requires careful design of the array structure and a fabrication process which can produce junctions with uniform parameters (I_c and R_J). This task could become quite difficult for arrays having a few hundred junctions. Fortunately, as a direct consequence of the advancement in Nb based superconducting circuits fabrication technology, the 1D array has reached the stage of being practical for many applications, especially those need compact mm and/or sub-mm wave sources capable of producing several tens of μW power.

D. Two-dimensional array

A natural extension to the concept of 1D array is a two-dimensional (2D) array as shown in Fig. 1(d). A 2D array of $N = M \times N_s$ junctions, where M and N_s are the number of junctions in a single column (a series element) and the number of series element, can be viewed as a 1D array of N_s junctions each having critical current MI_c and shunt resistance R_J/M. Hence, Eq. 3 and Eq. 4 can be applied to a 2D array by the following substitutions: $N \rightarrow N_s$, $R_J \rightarrow R_J/M$, and $R_d \rightarrow R_d/M$. In principle

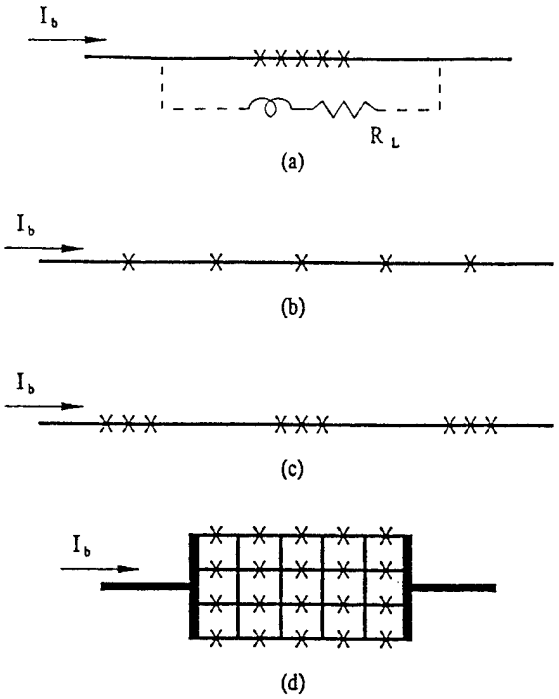

Fig. 1. Schematics of: (a) a 1D lumped array, (b) a 1D quasi-lumped array, (c) a 1D distributed array, and (d) a 2D array of $M = 4$ and $N_s = 5$. In (a) the part shown in dashed lines is the external coupling elements.

a 2D array has all the advantages of 1D array. In practice, however, due to the finite inductance of the SQUID loop connecting junctions in the same column, the upper frequency limit of a 2D array is the lesser of the superconducting gap frequency ($2\Delta_{Nb}/e\Phi_0 \sim 1.4$ THz for Nb) and $f_s = 1/(2\pi\sqrt{L_s C})$ where L_s and C are the inductance of the SQUID loop and junction capacitance. For typical junction and array parameters f_s is substantially lower than the gap frequency [5]. So far the performance of 2D arrays has been quite disappointing [9]–[11] (with the exception of linewidth [5]) mainly due to the difficulty of achieving mutual phase-locking. For instance, the highest power measured from 2D arrays is still more than a order of magnitude lower than that from 1D arrays. The highest operating frequency of any 2D array reported is also well below 300 GHz. In addition, the claimed higher tolerance of critical current nonuniformity [12] is misleading.

The table below lists the recent experimental results (rf power, linewidth etc.) of various types of Josephson oscillator from research groups around the world. Note linewidth results of [1], [13] were estimated from Eq. 4 using the measured dynamic resistance of the array. From these results and the discussions presented above, we feel that 1D array is one of the most promising type of Josephson oscillator for sub-mm applications, especially when high output power is required. Although it put more demands on the fabrication technology than FFO does it is certainly within the reach of present day Nb/AlO/Nb fabrication technology. As a matter of fact, power obtained from 1D array is 10 to 100 times of those from FFO and 2D array. In the next section the problems encountered in the design and fabrication of large 1D ($N \geq 100$) array and solutions to overcome these problems will be discussed. Results from our recent work on 1D array (the last row of the table below) will also be presented.

Type	f_c (GHz)	P (μW)	Δf (MHz)	R_L (Ω)	N	Ref.
FFO	305	0.5	1.4	32	1	[3]
FFO	450	~ 1	1	45	1	[4]
2D	150	0.4	0.013	2	100	[5]
2D	250	~ 1	-	-	$\sim$600	[10]
1D	370	7	1	26	40	[13]
1D	300	2	7	20	20	[2]
1D	400	50	0.17	68	500	[1]
1D	370	40	-	80	536	-

III. Development of 1D Array Oscillator

A. Theoretical background

There are several ways to obtain mutual phase-locking among all the junctions in a 1D array. The key is to have junctions interact with each other in a way such that all junctions oscillate in-phase. It has been shown that the most important phase-locking mechanism is the high frequency current (at the Josephson frequency) flowing through the junctions coupled globally by an inductive load [14], [15]. The structure of a globally coupled 1D array is shown schematically in Fig. 1(a). Based on perturbation theory [14], the equation which describes the time evolution of the junction phase and hence the time-dependent voltage across a junction in the array is given by:

$$\frac{d\varphi_k}{dt} = v_k^u + \alpha_k R_{dk} \sum_{m=1}^{N} \epsilon_m |Y_{km}| \cos[\arg(Y_{km}) + \delta\varphi_{km}], \tag{5}$$

where junction index k runs from 1 to N, φ is the gauge invariant phase, v^u is the dc voltage for an unperturbed junction at biasing current I_B, α is the so called down conversion coefficient, R_d is the dynamic resistance, ϵ is the amplitude of the voltage oscillation at the Josephson frequency. Y_{km} and $\delta\varphi_{km} \equiv \varphi_m - \varphi_k$ are the admittance matrix element and the phase difference between the kth and the mth junction, respectively. In Eq. 5 voltage is in units of averaged $I_c R_J$ of all N junctions. For a given 1D array configuration its phase-locking property can be investigated by numerically integrating Eq. 5. Figure 2 shows the result of the numerical simulations on two dif-

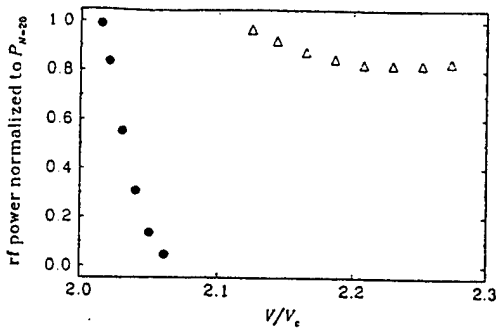

Fig. 2. rf power coupled to a matched load as a function of the junction voltage obtained by numerical simulations for two $N = 20$ junction arrays The solid dots are for the quasi-lumped array and the empty triangles are for the distributed array of $M = 5$

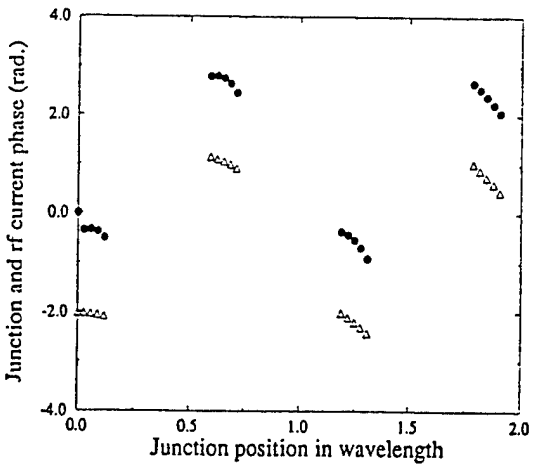

Fig. 3. Results of numerical simulations of an $N = 20$ and $M = 5$ distributed array. The solid dots represent the junctions' phases and the empty triangles are the phases of the rf current at each junction's location. The center-to-center distance between the adjacent junction groups is about 0.5λ.

ferent $N = 20$ 1D array structures: quasi-lumped and distributed array (defined later). It can be seen from Fig. 2 that the distributed array has a much greater frequency tuning range. We have carried out simulations for arrays having up to 200 junctions. The result confirms that distributed array is better in terms power, tuning range, and circuit density. The computing power required increases as N^2. Hence, simulation of arrays with $N > 200$ is practically difficult. Fig. 3 shows the phase variations among the junctions in the half-wavelength distributed array. Note that junctions within the same group have approximately the same phase, while the phases between two neighboring groups separated by about one half of a wavelength differ by about π. This phase arrangement results in a coherent combination of rf current flowing through the load. However, the structure is resonant in nature so that the frequency tuning range is still limited. A detailed analysis of phase-locking in 1D arrays can be found in [14] and [15].

B. Basic types of 1D array

Series 1D array may be classified into four basic types:

(1) The lumped array in which all junctions are close-packed within a distance of less than 0.1-0.2 λ to ensure a uniform phase among all junctions. This approach limits the total number of junctions to $N \sim 10$ and thus has limited output power.

(2) The compact array in which all junctions are closely packed while the total length of the array can be longer than a few wavelengths. In this way, a large number of junctions can be used to increase the output rf power level and reduce the linewidth. A 40-junction compact array has been demonstrated to produce ~ 1 μW power into a 15 Ω load in a wide frequency range (from 300 GHz to 500 GHz) [16]. The potential problem of this type of array is that some junctions may not phase-lock (as suggested by our numerical simulation) and lead to an increase of linewidth.

(3) The quasi-lumped array in which junctions are placed along a microstrip transmission line at a nearest neighbor distance of λ or $\lambda/2$. At operating frequency $f = \bar{c}/\lambda$, where $\bar{c}$ is the phase velocity in the transmission line, all junctions see the same impedance as if they are lumped together. The number of junctions in a quasi-lumped array can be very large. However, this design uses space inefficiently and has a narrow tuning range (see Fig. 2).

(4) The distributed array in which each junction in the quasi-lumped array is replaced by a group of M closely packed junctions. Each group occupies a linear space of much less than λ. For a given number of total junctions this design uses M times less space than a quasi-lumped array does. In addition, the tuning range is substantially increased from that of a quasi-lumped array.

C. Parameter optimization

Once the type of array has been selected the next step is to optimize junction parameters for a given application. First, the normalized operating voltage of the junction $v \equiv V/V_c$ should be about unity to obtain good waveform and strong phase-locking at the same time. This condition sets the characteristic voltage of the junctions to be $V_c \approx f_c\Phi_0$, where f_c is the center frequency of the band in which the oscillator is intended to operate. The number of junctions N is then determined from $N = \sqrt{8PR_L/V_c^2}$, where P is the desired output rf power. Each junction's resistance is chosen to be $R_J = R_L/N$ for maximum power efficiency. Finally, the critical current of the junction is

determined by $I_c = V_c/R_J = f_c\Phi_0 N/R_L = \sqrt{8P/R_L}$. For example, an application which requires $P = 100\ \mu$W, $R_L = 50\ \Omega$, and $f_c = 400$ GHz will need 250 junctions each with $V_c = 0.8$ mV, $I_c = 4$ mA, and $R_J = 0.2\ \Omega$. To obtain the formulas given above, it is assumed that the waveform is sinusoidal, the interconnection between junctions are lossless, and all junctions have uniform phase. In practice these assumptions are only approximate, e.g. waveform at $v \sim 1$ contains significant harmonics, interconnections have significant loss especially at frequencies close to $\Delta_{Nb}/e\Phi_0 \sim 700$ GHz, and phase variations among junctions are not always negligible. Taken these factors into consideration, one should use more junctions with higher critical current while keep V_c approximately constant by lowering R_J. Arrays designed and fabricated in this way should be able to produce the required power and narrow linewidth (see Eq. 4).

D. DC biasing scheme and parameter margin

For a 1D series array, the junctions are always connected in series in the high frequency equivalent circuit. However, the low frequency (dc) bias can be either parallel, series, or mixed. For the sake of simplicity only parallel and series dc bias will be discussed. Since the dc voltages of all junctions are the same in a dc parallel biased array, it can tolerate more critical current and shunt resistance non-uniformity. On the other hand, the total bias current of the array equals the sum of all junctions' bias current which can easily exceed several amperes and thus generate problems such as local heating. In contrast, the total current of a series biased array is the same as that of a single junction in the array which is usually less than 10 mA and is only $1/N$ times of current required for a parallel biased array. The voltage of the array is increased to approximately NV_c which is less than a volt even for an 800-junction array working at 600 GHz and can be handled with ease. However, non-uniform junction parameters impose more serious problem for 1D dc series biased array. It is obvious from Eq. 5 that junctions having different I_c with same the bias current tend to develop different voltages, *i.e.*, oscillate at different frequencies. If the difference in I_c is small, there is a good chance that the interaction between junctions via down converted high frequency current (represented by the second term in Eq. 5) can pull the otherwise different junction voltages into a common one. However, if the non-uniformity in I_c exceed some critical value this interaction will not be strong enough to pull the 'bad' junctions back. In general this critical value of non-uniformity (margin) depends not only on the number of junctions in the array but also on the arrangement of junctions' position in the array and hence has to be determined by numerical simulations. For an series biased array of 40 junctions we find that the margin in critical current is about 7% (1σ). Non-uniform R_J has a similar detrimental effect on phase-locking. In our earlier work parallel bias has been used to overcome the large spread in junctions' I_c and R_J [2], [13]. In recent years as a result of advancement in low-T_c circuit fabrication technology, especially since the successful development of the Planarized All Refractory Technology for low-T_c Superconducting circuits (PARTS) [17] and high-J_c Nb trilayers, the fabrication of large scale ($N \sim 500$) series biased array with less than 3% (1σ) spread in both I_c and R_J has been realized.

E. Experimental result

In an earlier publication [1], we have reported our result on 1D series arrays of 500-junction fabricated at IBM using AT&T trilayer. The measured maximum power coupled to a 68 Ω load was ~50 μW around 400 GHz and 10 μW around 500 GHz. The linewidth estimated from the measured dynamic resistance was less than 500 kHz, *i.e.* $\Delta f/f \sim 10^{-6}$.

Here, we present our recent work on 1D distributed arrays designed and fabricated in our laboratory. The arrays are all series biased with 4 junctions in each group ($M = 4$). Each array contains $N = 536$ or $N = 568$ shunted Nb/AlO/Nb junctions fabricated using a modified PARTS process. The measured critical current and junction resistance uniformity are better than 3% (1σ). The circuits were made on 5 cm diameter Si wafers and were diced into 6 mm × 6 mm chips before testing. Chips were mounted on 68-pin chip carriers and were tested in a shielded liquid helium dewar. Figure 4 shows the schematics of an $M = 4$ 1D array with a separation of one wavelength betwween two adjacent junction groups. Figure 5 is the photograph of a fabricated 1D array. The spacing between two adjacent junction groups is $\lambda/2$ at the center frequency.

Several samples have been tested for sub-mm wave generation. For each array, power coupled to the on-chip load resistor R_L was determined from a Josephson junction (the detector junction) used as a microwave detector placed directly after the load resistor (see Fig. 4). Figure 6 shows the detector's current-voltage characteristics ($I - V$ curve) with the radiation from the array oscillator. When the array is biased at 408 mV (*i.e.*, 0.761 mV per junction on average) a constant-voltage current step (the first Shapiro step) at 0.756 mV develops in the detector's $I - V$ curve (see Fig. 6). Within the resolution of our instrument, the step voltage of the detector junction is equal to the array voltage divided by N. The agreement between the detector's step voltage and the average voltage per junction in the array strongly suggests that all junctions in the array are phase-locked. The size of the first Shapiro step is used to determine the amplitude of the rf current I_{rf} flowing through the detector (and load). Due to the significant parasitic inductance associated with the external shunt resistor R_s, the detector has to be modelled by the resistively, inductively, and ca-

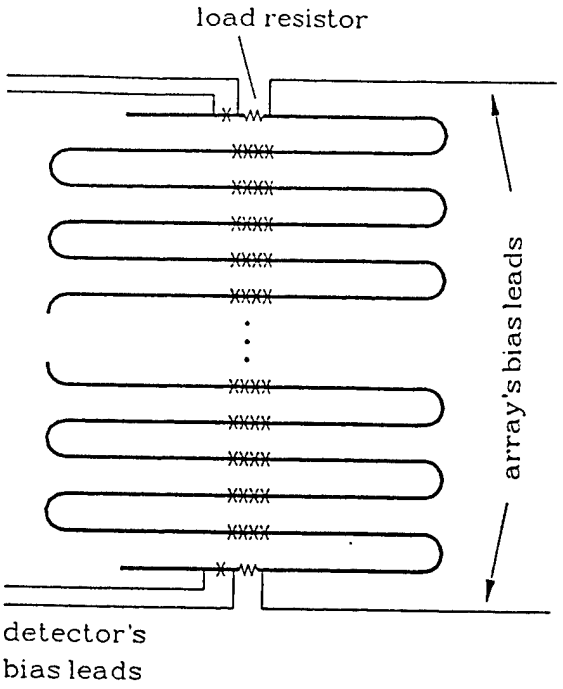

Fig. 4. Schematics of a distributed 1D array with its associated load resistors and detector junctions.

pacitively shunted (RLCSJ) junction model [18] (also see Appendix) rather than by RSJ model (use of RSJ model leads to an overestimate on I_{rf}). From the detector $I-V$ curve shown in Fig. 6, $I_{rf} = 1.0$ mA is obtained which results in 40 μW power coupled to the 80 Ω load resistor. As a comparison, the output power estimated from Eq. 3 using independently measured junction parameters ($I_c = 3.8$ mA and $R_J = 0.07\ \Omega$) is $P = 59\ \mu$W, assuming $\kappa = 1$. The difference in the rf power directly measured from the on-chip detector junction and that of calculated from Eq. 3 can be accounted for by the loss in the transmission line due to Nb's surface resistance, the imperfect phase alignment among junctions, and $\kappa < 1$ for the real device.

IV. Conclusion

The development of Josephson oscillators has reached a stage such as they could be used as sub-mm wave sources for applications where compactness is a necessity and moderate power levels are required. Josephson oscillators have been demonstrated to generate ~50 μW power into $\geq 50\ \Omega$ load in sub-mm frequency range (350 GHz - 450 GHz) with linewidth approaching a few hundred kHz. Frequency tuning seems the major remaining problem if a tuning range of greater than 25% of the center frequency and more than 10 μW output power are required simultaneously. The difficulty in increasing the tuning range has quite different roots for FFO and 1D array oscillator. Since a typical FFO's source impedance ($< 1\ \Omega$) is much lower than the impedance of a typical load ($\sim 50\ \Omega$) and the power generation capability is moderate (a few μW), it is necessary to use impedance transformers to couple enough power to a suitable load ($\sim 50\ \Omega$) which in turn limits its operational frequency range. The problem of impedance mismatching does not occur for 1D arrays since a 1D array's source impedance NR_J can be readily matched to the load impedance. However, the structure of 1D arrays (except lumped arrays) is resonant-like and hence the frequency bandwidth is also limited. One solution to this problem, providing that only moderate power (e.g. $\sim 1\ \mu$W) is needed, is by the use of a 1D array with 50 to 100 μW power at its center operation frequency and an integrated SIS attenuator [19]. This solution is adequate for applications which do not require oscillator's frequency to be rapidly tuned.

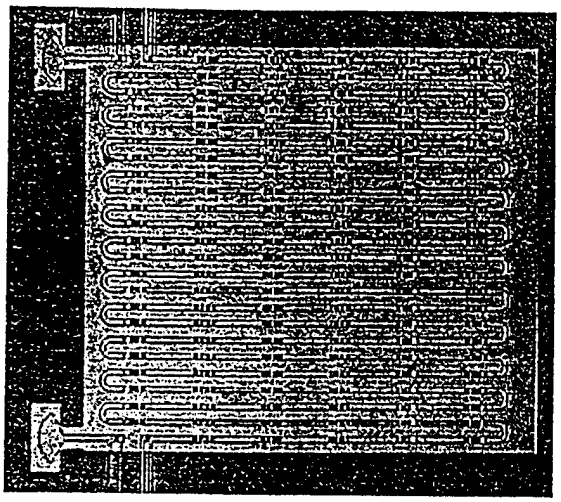

Fig. 5. A fabricated $N = 568$, $M = 4$ 1D array. The area occupied by this array is about 800μm by 800 μm.

One way to increase the output power of FFO is to use vertically stacked FFOs [20]. In principle when phase-locked, it should increase output power and reduce linewidth. However, the phase-locking mechanism of stacked FFOs is complicated and more researches are needed to increase our understanding on this issue. In the case of the 1D array, one way to increase its tuning range is to use a traveling-wave array [14] which does not use a resonant structure. In a traveling-wave array the required phase differences between the neighboring junctions for complete mutual phase-locking can be obtained by adjusting the amount of magnetic flux in the SQUID loops connecting the adjacent junctions.

In conclusion, Josephson mm and sub-mm wave sources have been improved dramatically over the past few years as a consequence of our increased theoretical understanding and fabrication capability. Although the present day Josephson oscillators have met requirement of some

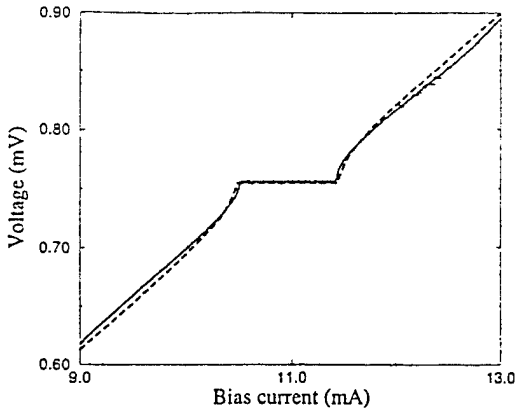

Fig. 6. Solid line: measured $I-V$ curve of the detector junction when the array was biased at 408 mV (N = 536). Dashed line: calculated $I-V$ curve using the measured junction parameters and I_{rf}=1.0 mA.

mm and sub-mm wave applications such as an on-chip integrated receiver for radioastronomy and atmosphere physics, further progress has to be, and can be, made so that their applications in many areas can be realized.

V. Acknowledgment

The authors thank A. Jain, K. Wan, and A.H. Worsham for their contributions in the early stages of this work.

VI. Appendix

A. RLCSJ model

Many applications such as dc SQUIDs, Josephson mixers, microwave detectors, digital circuits based on single flux quantum logic, and Josephson array oscillators require junctions with non-hysteretic dc $I-V$ characteristics. For low-T_c circuits this is usually done by placing an external shunt resistor R_s across a Nb/AlO/Nb tunnel junction (which seems to be the only type of Josephson junction reliable and reproducible enough for moderate to large scale superconducting integrated circuit applications). However, there is a parasitic inductance associated with the external shunt resistor due to its finite physical size. The existence of this parasitic inductance can lead to a significant change in the junction's dynamics. Hence, under many circumstances the use of the RSJ model [21] to describe such an externally shunted tunnel junction is inadequate and sometimes unacceptable [18] so that a more realistic junction model such as RLCSJ described below has to be used.

The equivalent circuit of an RLCSJ is shown in Fig. 7 in which R_t is the inverse of the intrinsic tunneling conductance and is in general voltage dependent. The dynamics

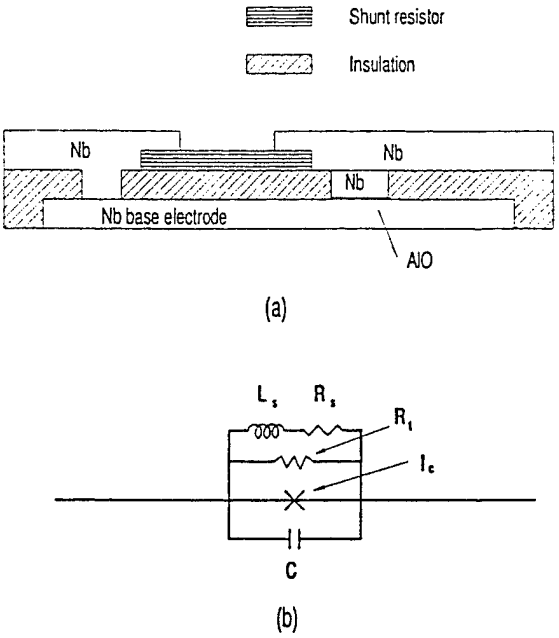

Fig. 7. (a) schematics of an externally shunted Nb/AlO/Nb tunnel junction, and (b) its ciruit model.

of such a junction are given by the following differential equations:

$$C\frac{\Phi_0}{2\pi}\frac{d^2\varphi}{dt^2}+\frac{\Phi_0}{2\pi}\frac{1}{R_t}\frac{d\varphi}{dt}+I_s+I_c\sin\varphi=I_B$$

$$L_s\frac{dI_s}{dt}+I_sR_s=\frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}$$

Where, R_s, L_s, and I_s are the resistance of, inductance of, and current flowing through the external shunt, respectively. I_B is the total bias current. The equations can be written in terms of normalized units as:

$$\beta_c\frac{d^2\varphi}{d\tau^2}+\alpha\frac{d\varphi}{d\tau}+\sin\varphi+i_s=i_B$$

$$\beta_L\frac{di_s}{d\tau}+i_s=\frac{d\varphi}{d\tau}$$

Where, $\beta_c\equiv 2\pi I_cR_s^2C/\Phi_0$, $\beta_L\equiv 2\pi L_sI_c/\Phi_0$, $\alpha\equiv R_s/R_t$, $i_s\equiv I_s/I_c$, $i_B\equiv I_B/I_c$, and $\tau\equiv(2\pi I_cR_s/\Phi_0)t$. In general I_B contains both the dc bias current and bias currents at high frequencies. For junctions with $R_t\gg R_s$ the second term in the first equation ($\alpha d\varphi/d\tau$) can be neglected. The dynamic behavior of an RLCSJ is much more complicated than that of an RSJ especially when both β_L and β_c are close or greater than unity.

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Appendix B

A Planarized Process for Low-T_c Electronic Applications

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Abstract - A low-T_c planarized process, with two Nb superconducting wiring layers in addition to the Nb/AlO_x/Nb trilayer, is described. The planarization of the first dielectric layer is carried out by using chemical-mechanical polishing. This planarization step and a combination of photolithography and electron-beam lithography has allowed us to fabricate Josephson junctions less than 0.01 μm^2 in area and enhance the performance of a variety of circuits and devices.

I. Introduction

In order to achieve the full potential of Josephson junction based devices, it is necessary to reduce the junction size and the area occupied by the associated circuitry by an order of magnitude from what is now commercially available. Planarization by chemical-mechanical polishing (CMP) and the development of PARTS (planarized all-refractory technology for superconducting electronics) was first carried out at IBM as a viable step to achieve the above goal [1]. CMP allows one to achieve global planarization and to meet the depth of focus requirements for fine-line lithography for subsequent layers. It also eliminates the need to open vias in the oxide to make contact to the junction counterelectrode (CE) so the junction size can be reduced to the deep-sub-micron regime.

At SUNY, we have incorporated electron-beam lithography (EBL) in the PARTS process to reduce the junction area by two orders of magnitude and added an additional wiring layer, a necessary requirement for many digital and analog circuits. The process steps for this PARTS process and the results on a variety of devices are described below.

II. PARTS Process

The process sequence is shown in Figure 1. First, a Nb/AlO_x/Nb trilayer is deposited on 2" diameter oxidized Si substrates in a cryopumped sputtering system with a base pressure of 1 x 10^{-7}Torr. The critical current density of the trilayers is varied from 1 kA/cm^2 to 300 kA/cm^2 by using oxygen exposures between 15,000 mT*min and 10 mT*min [2].

The next step in the process is the patterning and etching of the junction CE (M3). This is followed by the base electrode (BE) etch (M2), SiO deposition and planarization by CMP, contact via etch (I2), resistor deposition by lift-off (R1), first Nb wiring layer and etch (M4), second insulator deposition and contact via etch (I3)and finally the second Nb wiring layer deposition and etch (M5). In some circuit applications, an additional Au film is deposited on the contact pads by the lift-off technique. A description of these layers, layer thicknesses and minimum linewidths are shown in Table 1.

For defining junction sizes less than 1.0 μm, the etch mask for the Nb counterelectrode is patterned by EBL. A bilayer resist of P(MMA, MAA) and PMMA which is sensitive to both electron-beam and DUV light is used in this case [2]. After e-beam exposure, a 50 nm thick layer of SiC is deposited, lifted-off and used as an etch mask. For one micron, or larger, junctions and for all other layers requiring etching, (Nb and SiO) patterning is done by photolithography using S1813 photoresist and a contact mask-aligner with a DUV light source. The lift-off mask for resistors consists of AZ-5214E photoresist.

Nb films are etched in a reactive-ion-etcher in SF_6 plasma. An end-point detection scheme based on the optical emission intensity of a selected fluorine line allows timely termination of the etching process. For etching vias in SiO, a mixture of CHF_3 and oxygen is used.

Table 1. PARTS Process Layer Description

Layer Name	Thickness (nm)	Min. Width (μm)
M3	100 - 150	0.1
M2	150	0.8
I2	130	1.6
R1	30 to 80	1.0
M4	200	0.8
I3	300	1.6
M5	400	1.2
Au	50	2.0

Either electron-beam evaporated Au or PdAu is used as the resistor material. The sheet resistance range for Au is 0.5 to 1 Ω/□ and 4 to 20 Ω/□ for PdAu. The minimum resistor linewidth is 1 μm.

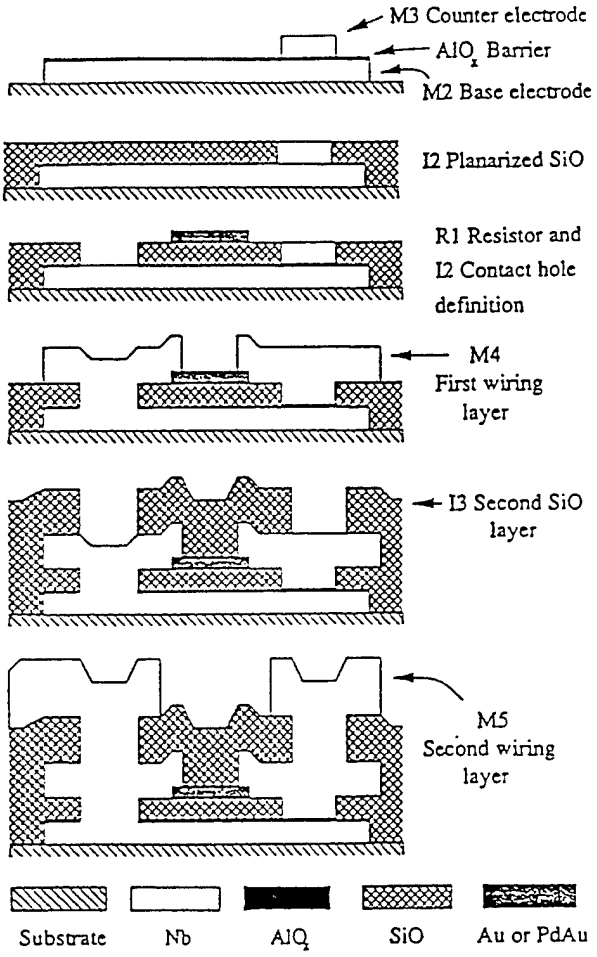

Figure 1. PARTS Process Flow Description

III. Chemical-Mechanical Polishing

CMP, the key step in this process, is carried out on a commercial polishing machine. The polishing pad is IC-1000 and the polishing slurry is ILD-1300, both from Rodel Corp. The hard IC-1000 polishing pad can planarize wider features more effectively than the softer SUBA-500 and SUBA-IV pads [3]. The polish rate uniformity across the wafer is better than +/- 5%. The end-point in the CMP process, reached when the top surface of the Nb CE is exposed, is confirmed both by visual inspection and surface profile.

In a commercial CMP process, the load is applied to the wafer and the relation between the oxide removal rate, R , and the pressure, P and the relative velocity between the wafer and the polishing table, V is given by

$$R = k\,PV \qquad (1)$$

where k is a constant related to the mechanical properties of the oxide and the polishing pad.

In our work, we have found a new polishing regime where the wafer is only in partial contact with the asperities of the pad. This is achieved by distributing the load between the wafer and the substrate mounting assembly by increasing the pocket depth of the substrate template. In this polishing regime, the oxide removal rate remains constant over a wide range of applied loads (20 to 160 lbs) and relative velocities (0.6 to 16 m/s) and is independent of the pad surface condition. The removal rate is only a function of the silica content in the slurry, a rate as high as 232 nm/min can be achieved with a 6.5% silica concentration. In order to terminate the CMP within 20 nm of the end-point, the slurry is diluted with DI water to achieve a rate of 60 nm/min. This modified CMP process has a high run-to-run reproducibility and the planarization takes place in a single CMP step.

In the process sequence described above, the second wiring layer is used as the ground plane. This restriction is applied since, in CMP, large metal features planarize at a slower rate.

IV. Device Fabrication Using All-Photolithographic Process

Submillimeter wave sources based on series biased distributed Josephson array oscillators have been fabricated using this PARTS process. Arrays containing 480 shunted junctions, with a critical current I_c of 3 mA (corresponding to a J_c of 50 kA/cm^2) deliver rf powers up to 50 μW to an 80 Ω on chip load at 400 GHz. The uniformity in I_c across the array was better than +/-3% which is an important condition for achieving phase-locking among all the junctions. The power was determined from the size of the Shapiro step of the on-chip Josephson junction detector. Series biased linear arrays making use of the highly uniform, small size junctions fabricated with PARTS process should be capable of generating sub-millimeter wave powers in the milliwatt range.

A T Flip-Flop, fabricated using the PARTS process (with a single junction size of 1.5 μm and a J_c of 6.5 kA/cm^2), operating up to an input pulse frequency of 370 GHz has been reported earlier [4]. In this first version of an RSFQ circuit, only one Nb wiring layer was used and the layout

was modified to minimize the parasitic inductances. For more complex RSFQ circuits, it is necessary to add another superconducting wiring layer acting as a superconducting ground plane. Fabrication and successful operation of some simple RSFQ circuits, such as the T Flip-Flop, DC/SFQ - SFQ/DC converter and an inverter circuit, using this additional layer has now been demonstrated.

V. Device Fabrication Using EBL

Single junctions and series array of junctions ranging in size from 0.1 to 6 μm were fabricated with EBL junction definition [2]. Figures 2(a) and (b) show the I-V characteristics of two Josephson junctions with J_c's of 2 kA/cm^2 and 30 kA/cm^2 respectively.

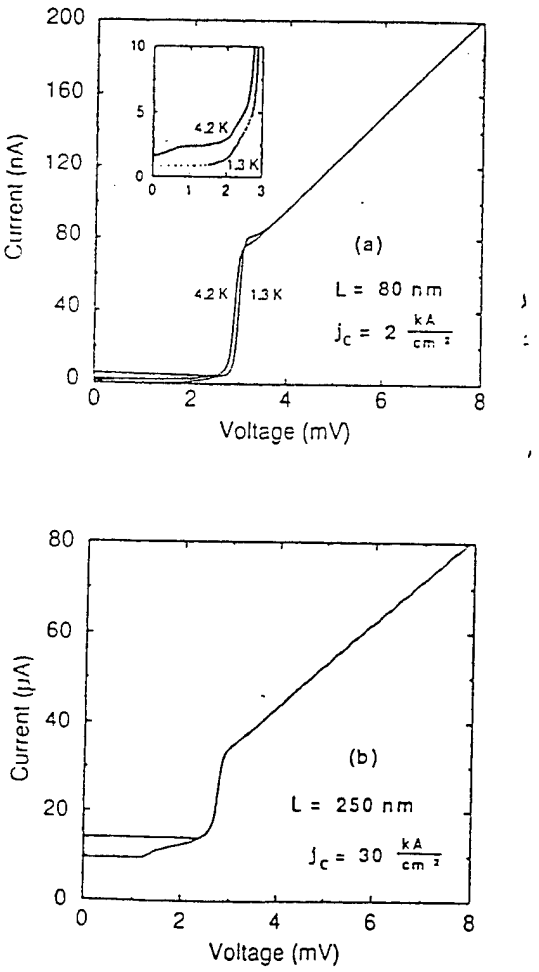

Figure 2 (a) and (b). I-V characteristics of Josephson junctions (a) size - 0.08 μm, (b) size - 0.25 μm.

A variety of washer SQUIDs, susceptometers, magnetometers and gradiometers [5] have been fabricated with junction sizes from 0.2 to 1.0 μm. The J_c's were selected to be 2 kA/cm^2 to 50 kA/cm^2 to maintain a critical current of 20 μA. Reduction in junction size allows us to increase the I_cR product and to improve the noise performance. It is predicted that such SQUIDs can operate in high magnetic fields and achieve an energy sensitivity near h [5].

VI. Conclusions

We have established a planarized process modeled on PARTS for the fabrication of low T_c circuits using eight levels of lithography. Devices with a minimum junction size of 1 μm are made using DUV lithography. With the addition of EBL, high quality junctions with dimensions of less than 0.1μm for J_c ranging from 1kA/cm^{2}to 300 kA/cm^2 have been obtained.

Acknowledgments

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Chemical-Mechanical Polishing in Semidirect Contact Mode

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ABSTRACT

In a typical chemical-mechanical polishing (CMP) process for interlevel dielectric planarization, the oxide removal rate is strongly dependent on the parameters such as applied load, relative speed, and pad surface properties. However, the experimental results presented in this work show that by maintaining a thin fluid film between the pad and the wafer and thereby reducing the role of the asperities in the pad, the oxide removal rate can be made independent of these polishing parameters. In this semidirect contact mode, the CMP process, carried out on 2 in. wafers, resulted in a uniform polish rate across the wafer, high run-to-run reproducibility, high selectivity between materials of differing chemical properties, and eliminated the need for pad surface conditioning and *in situ* end-point determination equipment.

Introduction

Chemical-mechanical polishing (CMP) has been in use for optical finishing of glass and Si surfaces for many decades.[1] Application of CMP for the planarization of interlevel dielectric (silicon oxide) as well as for polysilicon and tungsten metal studs was pioneered by IBM and has been used in the fabrication of very large scale integrated (VLSI) circuits since 1985.[2,3] It has now emerged as the most effective method of achieving global planarization in multilevel circuits with feature sizes less than 0.5 μm, in order to meet the shallow depth-of-focus requirements of optical projection lithography equipment.[4] Although this technology has been mainly developed for Si integrated circuit (IC) manufacturing, its use has now been extended to other thin film circuits where small feature sizes and multilayer interconnections are required.[5]

CMP is carried out by pressing a rotating wafer against a moving polishing pad on which a suitable slurry is dispensed. For oxide polishing, the slurry consists of silica particles dispersed in an aqueous solution. The oxide surface is chemically modified, and this modified layer is removed by mechanical action. As the removal rate is a function of the height of a feature in relation to its surroundings, CMP reduces the surface topography, producing highly reflecting surfaces. This phenomenon is utilized in IC fabrication, where processing of multilayers produces surface irregularities such as steps at the edges of the layers and depressions where contact is made to an underlying layer.

In spite of its heavy use in VLSI manufacturing, a limited information on the role of various CMP parameters such as pressure, relative velocity between the pad and the wafer, mechanical properties of the pad and the oxide, temperature, chemical reaction rate, and slurry flow distribution, is available in the open literature. Theoretical modeling of such a complex system has so far only been done based on simple mechanical models.[6,7] While altogether neglecting the chemical reactions in the process, the models do not even take into account the full range of mechanical and hydrodynamic parameters such as surface roughness of the pad, pad-wafer contact area, slurry flow pattern, and the residence time of slurry particles on the wafer.

In general, CMP does not provide good selectivity between different materials, making it difficult to determine the end point in this "blind" experiment. A high run-to-run reproducibility and a uniform polish rate across the wafer are therefore very desirable for a timely termination of the process. Usually a trial and error method is adopted to obtain the most suitable polishing conditions for a specific application. In manufacturing, the process is qualified by employing statistical methods to determine the effect of process variables. These techniques require that a large number of experiments be conducted for each specific tool and application. The entire procedure is therefore time consuming and expensive but essential for a successful application of CMP. It is no surprise that, so far, only large organizations have been able to utilize this process to their advantage and most of the experimental details are proprietary.

In this work, an empirical approach is adopted to demonstrate the solid-solid and solid-fluid interactions in CMP, as applied to interlevel dielectric planarization (ILD). This is accomplished by suitable modifications of the wafer mounting assembly, which changes the pad-wafer contact and the fluid flow distribution across the wafer. A brief theoretical background describing the existing models for CMP is given and the appropriate references cited. In the experimental data presented here, when the wafer is in partial contact with the pad, the oxide removal rate is found to be independent over a wide range of process parameters such as pressure, relative velocity, and pad surface properties. The experimental procedure for realizing these conditions may be dependent on the specific polishing equipment and wafer size. The main object of this work, however, is to demonstrate a robust CMP process, relying on the chemical reactivity of the oxide, for achieving a uniformly high removal rate across a wafer. In addition, this process provides effective planarization for ILD applications. The experiments reported here were carried out on 2 in. diam Si wafers with silicon oxide as the dielectric layer. A planarization process, similar to the multilevel metallization process used in VLSI fabrication, was developed for the fabrication of Nb-based superconducting circuits.

Theoretical Background

CMP relies on both the chemical reaction of the slurry with the oxide surface and a mechanical action for removing the reacted species, which distinguish it from chemical etching (solid-liquid interaction) and grinding (solid-solid interaction). The first mechanical model for CMP, proposed by Preston in 1927, empirically related the removal rate, which is the average change in the thickness per unit time, to the work done by the tangential frictional force exerted by the pad on the wafer. The removal rate, R, is given by the well known Preston's equation

$$R = K_p v F/A \qquad [1]$$

or

$$R = K_p v P$$

where F is the load applied to an area A, P is the pressure, v is the relative velocity between the pad and the wafer, and K_p is a constant proportional to the coefficient of friction.[6] Later the model was expanded by others to include the surface interactions between the silica particles and the asperities in the polishing pad and the oxide.[8,9] Because of the high local pressure at the points of contact, the oxide surface undergoes an elastic/plastic deformation and the material is removed by a grinding action as these particles are dragged along the surface. The penetration depth of the particles is calculated to be less than 1 nm, confining the interaction range to approximately a monolayer on the surface. The rate of material removal, R, defined by Eq. 1 is determined by the surface area of the silica particle in con-

tact with the wafer, and hence the applied pressure and the elastic properties of the silica particles, giving

$$K_p = 1/2\ E \quad [2]$$

where E is the Young's modulus of elasticity for silica. In another report, Tai-Kwan *et al.* have related K_p to the elasticity of the pad.[9] In reality, K_p is a function of a number of parameters, such as the elastic properties of the oxide and the pad, contact area between the pad and the wafer, and to a small extent the applied load and relative speed. As P changes with the contact area between the pad and the wafer, accumulation of dried silica particles on the pad and pad glazing may result in a decrease in removal rate.[10] Also, as the rate is a function of pressure, an uneven pressure distribution gives rise to nonuniformities in oxide thickness across the wafer after CMP.

Preston's equation is valid only in the limited regime where the pad is in direct contact with the wafer and does not cover all polishing scenarios. At high velocities, the wafer may glide on the pad at an angle, with a thin layer of slurry separating the two solid surfaces. The load is entirely supported by the fluid pressure built in this converging fluid film. A fluid-based model, using the principles developed for hydrodynamical lubrication of bearings, has been described in detail by Runnels.[7] This simple model assumes that the pad and the wafer are planar surfaces in relative motion, separated by a wedge-shaped film of slurry, which is an incompressible viscous fluid under laminar flow. The thickness of the fluid layer, h, in this tribological model for plane slider bearings is given by[11]

$$h = K_h\ (uv/PA)^{0.5} \quad [3]$$

where u is the kinematic viscosity of the slurry, and K_h is a constant. The fluid layer thickness where polishing occurs has been calculated under these assumptions to be in the range of 60 to 100 μm. [6] The exact calculation and measurement of the fluid layer thickness is a complex task, as in reality the pad surface is rough with height variations of the same order as the fluid layer thickness. The surface roughness of the pad, y, is defined as the standard deviation of the height of the asperities in the pad.[9] The two solid surfaces are completely separated by the fluid layer when $h >> y$ and are in partial contact when $h < 3y$. [11]

The chemical interactions in CMP must be considered as well. For a review of chemical processes in glass polishing, see Ref. 1. It is proposed that the water in the slurry chemically reacts with the silicon oxide, the reaction given by

$$\equiv Si—O—Si\equiv + H_2O \rightarrow 2\ \equiv Si—OH \quad [4]$$

The diffusivity of water in silicon oxide being low, only the molecules on the surface of the wafer and the silica particles in the slurry participate in this reaction. Hydrogen bonding occurs between the hydroxylated molecules on the two surfaces and these are carried away by the moving silica particles where a reverse of reaction 4 may take place. A fresh surface layer is then exposed, ready for the reaction to continue. The reaction rate is found to increase with temperature (increasing the diffusion coefficient of water), and the pH of the solution. The pH of the slurry is adjusted between 9.7 and 11 to obtain acceptable removal rates.

A model describing the removal rate must include all aspects of the polishing action. As an example, at very high pressures, the removal rate may actually decrease, because of an inadequate supply of slurry reaching the wafer surface and Preston's equation is not obeyed. On the other hand, as the fluid layer thickness increases with increase in velocity, the removal rate decreases because the contact area is reduced and the modified surface is not removed efficiently. The task is further complicated by the fact that the chemical reactivity at the oxide surface is affected by the hydrostatic pressure which is in turn related to the applied load and velocity.

Planarization occurs when the material on the features extending above the surface is removed faster than flat regions (field) and the material in the depressions is removed at a slower rate. In the ILD application described here, only protruding features are present. The process is sensitive to the pattern density, as isolated features planarize faster than clusters in which the planarization rate is affected by the neighboring features.[12,13] A phenomenological model for planarization was first developed by Warnock.[14] It assumes that the planarization rate is directly proportional to the feature step height and that this differential exists over a length scale over which the pad deforms. The predicted planarization rates for patterns of varying widths and spacings correlate well with the experimental data. The model also agrees with the experimental observation that harder pads planarize wider features more effectively than softer pads. With an increase in applied load, the deformation length as well as the planarization rate decrease. A discrepancy between the model and the experimental observation appears at the edges of an array of features which are polished at a faster rate than predicted. A fluid erosion based model proposed by Runnels takes into account the normal and tangential shear forces in the thin fluid film between the pad and the wafer.[15] This model predicts a lower planarization rate for larger values of h.

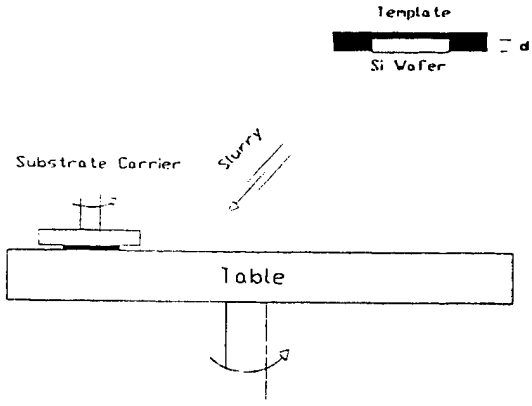

Fig. 1. Schematic of the CMP equipment, inset shows the template assembly.

Experimental

The wafers used in our experiments were 2 in. in diameter with thicknesses of 11 and 20 mils. Blanket (featureless) wafers were used for studying the dependence of oxide removal rates on the polishing parameters. The oxide films were either thermally grown quartz (SiO_2) or thermally evaporated SiO. The two oxides have different chemical properties, SiO being more chemically reactive than SiO_2. The refractive indexes of the SiO_2 and SiO are 1.46 and 2.0, respectively.

CMP was carried out on a Model 6CA Strausbaugh polisher. A scheme illustrating the essential features of this single-wafer CMP equipment is shown in Fig. 1. The wafer carrier and the table rotational speeds are controlled independently, and a small lateral motion is provided to the substrate carrier to reduce pad wearing. The wafer carrier and the water-cooled table on which the polishing pad are mounted are both rotated in the same direction to maintain a constant relative velocity at all points of the wafer.[16] The wafer is mounted on a template assembly for a single 2 in.

Table I. Properties of polishing pads (Rodel Corp.)

Pad	Hardness (a.u.)	Compressibility (%)	Density (kg/m³)	Roughness (μm)
Suba IV	57	17	300	30
Suba-500	70	7	350	22
IC-1000	100	2 to 4	640 to 740	12

Table II. Properties of polishing slurries for ILD planarization.

Properties	SC-1 (Rippey Corp.)[a]	ILD-1300 (Rodel Corp.[b])
Base	KOH	NH_4OH
pH	10.0 to 10.3	10.7
Specific gravity	1.198	1.07
w/o SiO_2	30 ± 0.3	13
Viscosity (kg/m-s)	<0.15	0.004

[a] Rippey Corp., Product Catalogue, El Dorado, CA.
[b] Rodel Corp., Newark, DE.

diam wafer. It comprises a 1 in. wide retaining ring to guide the wafer and a soft backing consisting of a buffed poromeric film laminated to Mylar (DF-200 from Rodel Corp., Newark, DE). The wafer is wetted and held in this template by surface tension. In typical CMP applications, the pocket depth of the template is chosen to be approximately two-thirds of the wafer thickness, to ensure intimate pad-wafer contact. In the set of experiments described here, pocket depths of 7, 9, 11, and 15 mils are used for wafer thicknesses of 11 and 20 mils, to modify the pad-wafer contact and the fluid flow distribution. The wafer-to-wafer variation in thickness was specified by the manufacturer to be ±1.0 mil. The measured values of wafer thicknesses were within ±0.5 mil.

The properties of the polishing pads, used in these experiments are listed in Table I. The pads were selected specifically to study the effects of their mechanical properties on the polish rate and the pattern sensitivity in the planarization process. The softer SUBA pads are constructed of polyurethane impregnated polyester felts, typically used for polishing Si surfaces. The IC pads are harder and consist of microporous polyurethane. Two different slurries, SC-1 and ILD-1300, were used to study the effect of particle size on oxide CMP. The properties of these slurries are listed in Table II. The slurries were diluted with deionized water to change the silica concentration. The oxide thickness, measured using an ellipsometer, was averaged over nine different locations on the wafer, to determine the removal rate on blanket wafers. The step height of a feature was measured on a profilometer with a 12.5 μm diam mechanical stylus tip.

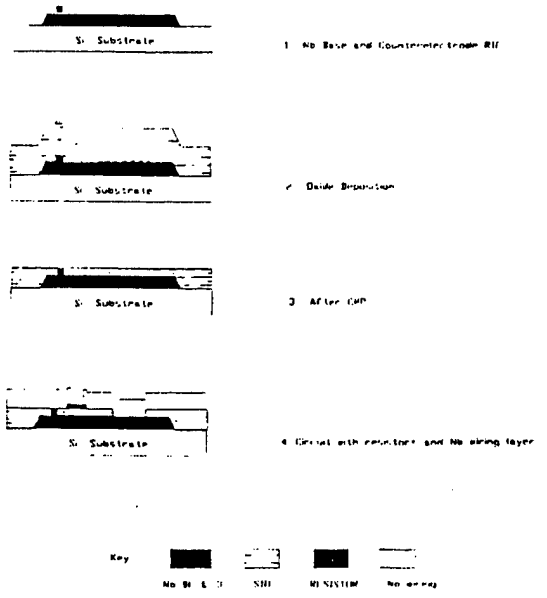

Fig. 2. Process flow diagram for the fabrication of superconducting circuits using CMP.

The planarization of features with varying widths and pattern density was carried out as part of the fabrication process for defining Josephson tunnel junctions in superconducting circuits.[17] The process steps are shown in Fig. 2. The tunnel junctions consist of two superconducting films (Nb) separated by a ~2 nm thick insulating barrier (AlO_x). CMP is used to planarize the dielectric layer (SiO) and polishing is continued until the tops of the junction counterelectrodes are clear. Contact is made to the exposed counterelectrode via another Nb wiring level. The process is similar to that used in interlevel dielectric planarization in VLSI multilevel interconnects. The film thicknesses of the Nb base and counterelectrodes are ~150 nm each and the SiO thickness, before CMP, is 600 nm. The planarization of the surface with step heights of 300 to 350 nm is carried out by removing approximately 300 nm of field oxide. The field oxide removal rate is adjusted to about 60 nm/min. As the counterelectrode is thin, the polishing must be terminated within ~20 nm of the end point to avoid weak links or shorts at the Nb-silicon oxide edge. A high run-to-run reproducibility in removal rates allows us to complete the CMP process in one attempt for a total polish time of around 5 min. After polishing, the wafers are cleaned by ultrasonic agitation in a NH_4OH solution followed by an isopropyl alcohol and DI water rinse to remove the slurry particles from the surface. This process has been utilized in the fabrication of deep submicron Josephson junctions and of digital and analog circuits operating at several hundred GHz.[18,19]

Results

Oxide Removal on Blanket Wafers

Oxide removal rates of SiO_2 and SiO were measured on wafers with thicknesses of 11 and 20 mils. A marked difference in the removal rate and its dependence on process parameters is observed with different template pocket depths. We believe that by increasing the pocket depth in relation to the wafer thickness, the ratio of solid-solid to solid-fluid contact areas on the wafer is decreased. This appears to bring about a change in the dominant mechanism in the CMP process, as is discussed later. The experiments are divided in three categories, based on the nature of the contact between the pad and the wafer. In the direct contact mode, the wafer is firmly pressed against the asperities in the pad. In the gliding mode, a thin film of fluid separates the pad and the wafer. In the intermediate regime, or semidirect contact mode, the fluid layer is sufficiently thin to allow a fraction of the pad asperities to come in contact with the wafer. At any given instant, the wafer is partially in contact with the fluid and partially with the pad asperities. The bulk of the data reported here lies in this intermediate regime. It is to be noted that because of the compressibility of the template backing, the true difference in the wafer thickness, t, and the pocket depth, d, is not known. The values of t and d presented here, are those specified by the manufacturer, and no attempt is made to preselect the wafers and the templates.

1. Direct contact mode: $(t - d) > 4$ mils.—This is a typical situation present in most CMP applications where the pocket depth is less than or equal to two-thirds of the wafer thickness. The removal rate is plotted as a function of applied pressure for SiO_2 and SiO in Fig. 3 for 20 mil thick wafers polished on IC-1000 (perforated) pads using an 11 mil template pocket depth. The slurry is SC-1, diluted to yield 2.4 weight percent (w/o) silica. The removal rates of SiO_2 and SiO are found to be comparable and the rates increase with pressure, following Preston's equation. The oxide thickness after polishing is nonuniform across the wafer, often producing a bull's-eye pattern, with the rate increasing with the radial distance. Similar results are obtained for 11 mil thick wafers placed in a template with a pocket depth of 7 mils, with somewhat improved uniformity. Only a limited number of experiments were done because of poor run-to-run reproducibility and thickness nonuniformity. The purpose of this set of experiments was

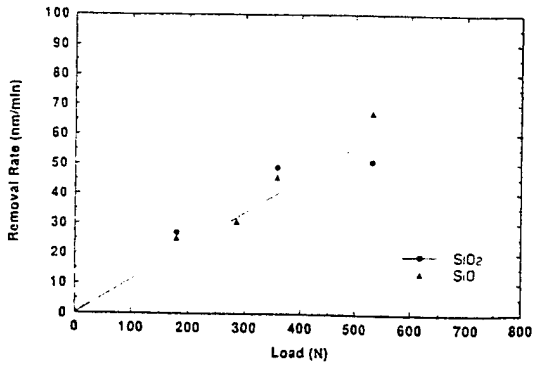

Fig. 3. Removal rates of SiO_2 and SiO as a function of applied load (t = 20 mils, d = 11 mils, v = 0.83 m/s, IC-1000 pad, SC-1 slurry with 2.4 w/o silica).

mainly to demonstrate the difference between the direct and semidirect contact mode.

2. Gliding mode : $t < d$.—When an 11 mil thick wafer is placed in a 15 mil deep pocket, the oxide removal rate is unmeasurably small (<1 nm/min). In this case it appears that the even though the wafer is well wetted by the slurry, in the absence of any direct contact between the pad asperities and the wafer, the oxide layer is not removed. The experiment demonstrates the necessity of the mechanical action performed by the pad.

3. Semidirect contact mode: $0 < (t - d) < 4$ mils.—In this case, the results are dramatically different than in the other two modes. The major results are described as follows. When an 11 mil thick wafer is placed in a template with a pocket depth of 9 mils, the removal rate is found to be independent of polishing parameters and pad properties. The removal rates of SiO_2 and SiO are compared to show the importance of chemical reactivities of the oxides. This is followed by experiments to show how the removal rate is affected by moving the wafer closer to or away from the pad. These experiments, in which the load may be supported by both the wafer and the template, describe the limits within which CMP is well behaved.

Case 3a. $(t - d) = 2$ mils.—The removal rate for SiO_2 on 11 mil thick wafers was measured using two different slurries. Table III shows the rates on IC-1000, SUBA-500- and SUBA-IV pads for different values of applied load and relative velocities. The data presented in Table III are highly reproducible and independent of the age of the pad. It is clear that the removal rate is only a weak function of applied load and velocity, and Preston's equation is not obeyed. As an example, on IC-1000 pad, increasing the Fv product by a factor of 12, the removal rate changes by only a factor of 1.6. Similar results are obtained on SUBA IV and SUBA-500 pads for relative velocities of 0.50 to 1.60 m/s and applied loads of 133 to 587 N. The rates on IC-1000 and

Table III. Removal rates of SiO_2 (t = 11 mils, d = 9 mils).

Pad	Slurry	w/o Silica	Relative speed (m/s)	Load (N)	Rate (nm/min)
IC-1000P	ILD-1300	3.3	0.58	133	35.9
			0.58	587	54.5
			0.83	360	46.2
			0.83	360	46.0
			1.65	133	36.9
			1.65	587	62.2
Suba IV	SC-1	3.0	0.50	133	39.2
			0.83	133	47.8
			0.83	360	50.9
			1.65	360	48.5
			1.65	360	48.1
Suba-500	SC-1	2.4	0.83	467	31.0
			0.83	587	42.7

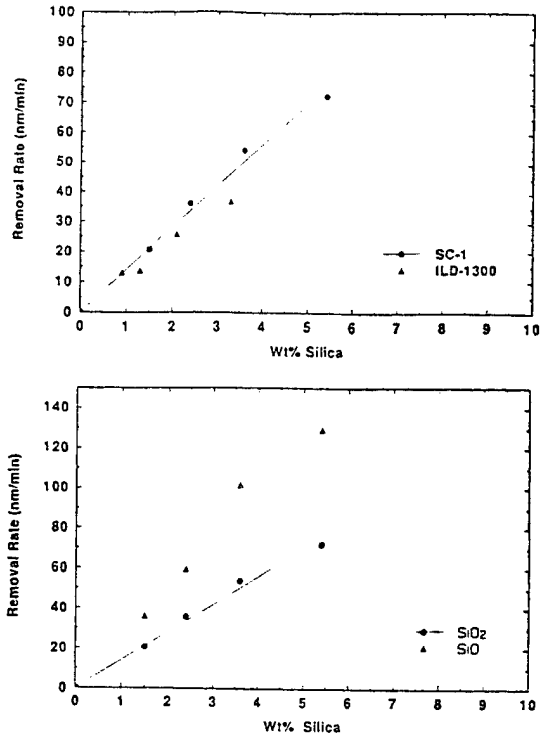

Fig. 4. Removal rates of (a, top) SiO_2 and (b, bottom) SiO_2 and SiO as a function of solid contents of the slurry (t = 11 mils, d = 9 mils, F = 360 N, v = 0.83 m/s, IC-1000 pad).

SUBA-IV pads are comparable even though their compressibility ratio is typically 6, and one might expect a large change in K_p.[9]

On the other hand, at a fixed load and velocity, the removal rate is a strong function of the solid contents of the slurry. In Fig. 4a, the rates for SiO_2 are plotted as a function of w/o silica for SC-1 and ILD-1300 slurries. The rates are found to be comparable for the two slurries.

The removal rate of SiO on SUBA IV, SUBA-500 and IC-1000 pads is again found to be a very weak function of F in the range of 133 to 580 N and v in the range of 0.58 to 1.65 m/s. However, the removal rates for SiO_2 and SiO are different by approximately a factor two as shown in Fig. 4b. The data shown here are for IC-1000 pad, but the same difference in the rates was found on the SUBA-IV and SUBA-500 pads and using both SC-1 and ILD-1300 slurries. The difference in the rates for the two oxides appear to be related to their chemical strengths, indicating that in this regime, the chemical reactivities of the oxides play a more important role than in the direct contact mode.

The effect of the pad surface appears to be relatively minor. This is exemplified by the observation that the rate does not change with pad usage. The effect is most noticeable on IC-1000 pad where the rate is reported to decrease when polishing 8 in. diam wafers, by as much as 30% in the first 20 min of polishing time.[19] In our experiments, we do not observe any change in the removal rate for over 300 min of polishing on the same IC-1000 pad. Since the relative velocities are high and the outward slurry flow (due to centrifugal force) is not impeded by the pad-wafer contact, the slurry particles do not settle and dry on the pad, maintaining the pad surface conditions constant and increasing the life of the pad.

The oxide thicknesses across the wafer before and after CMP, using IC-1000 pad and SC-1 slurry, are shown in Fig. 5. The rate is higher at the edges, the width of this rim being ~3 mm. The thickness uniformity across the wafer, excluding the edges is ±2%. Similar results were obtained

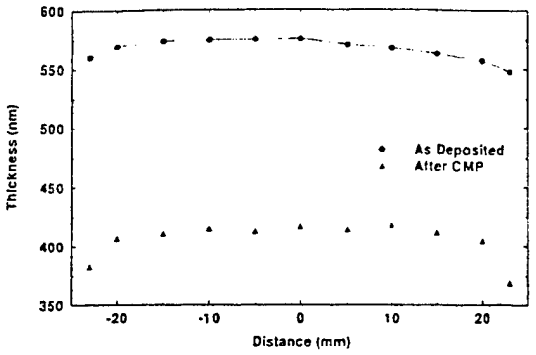

Fig. 5. SiO_2 thickness across the wafer before and after CMP (t = 11 mils, d = 9 mils, F = 360 N, v = 0.83 m/s, IC-1000 pad, SC-1 slurry with 3.0 w/o silica).

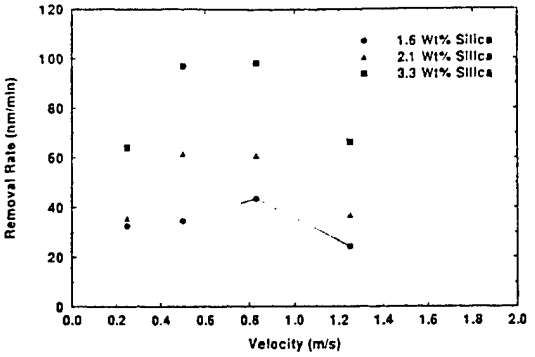

Fig. 7. Removal rate of SiO_2 as a function of velocity (t = 11 mils, d = 11mils, F = 360 N, IC-1000 pad, ILD-1300 slurry).

for SUBA-IV and SUBA-500 pads over the range of parameters shown in Table III.

Equation 3 predicts a change in fluid layer thickness with F and v. As the layer thickness is reduced, it is expected that the pad-wafer contact area is increased and the polishing action is described by Preston's equation. This behavior is apparent from Fig. 6a and b where the removal rate for SiO_2 is plotted as a function of velocity and applied load, respectively. When v is reduced below 0.30 m/s the removal rate decreases correspondingly with no polishing action taking place on a stationary wafer. Again, when the load is increased beyond 580 N, the removal rate increases sharply. The rate decreases at still higher loads, because of inadequate slurry supply. The limits of F and v, outside of which the rate begins to change appreciably are somewhat dependent on the mechanical properties of the pad, the boundaries being wider for a hard pad.

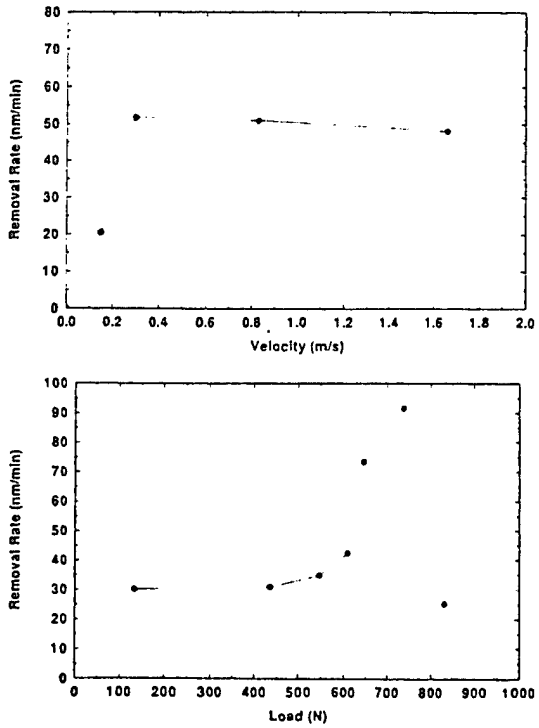

Fig. 6. Removal rate of SiO_2 as function of (a, top) velocity on SUBA IV pad for F = 360 N and (b, bottom) load on IC-1000 pad for v = 0.83 m/s (t = 11 mils, d = 9 mils).

Case 3b. $(t - d) = 0$.—When the pocket depth is increased, the limits over which the removal rate remains constant are considerably narrowed. In this case, the fluid layer thickness is increased, reducing the pad-wafer contact area compared to the previous case. The removal rate for SiO_2, as a function of relative velocity is shown in Fig. 7 for different silica concentrations. A qualitative explanation of the data is given as follows. At a low silica concentration of 1.6 w/o, the rate is relatively independent of v. At higher silica concentrations. the rate begins to decrease at velocities exceeding 0.80 m/s contrary to Case 3a. This may be because of an increase in fluid layer thickness at high velocities, reducing the pad-wafer contact area still further. The mechanical action of the pad then limits the removal rate. The rate is proportional to the silica concentration in the 0.30 to 0.80 m/s range, as in the case of the 9 mil pocket depth. At 6.5 % silica concentration, the measured rate for SiO_2 is 232 nm/min. The thickness uniformity across the wafer excluding the edge, is again ±2%, however. the width of this rim is about 1 mm, less than in Case 3a. This observation is in agreement with the other results, showing that the slurry flow is impeded as the pad-wafer contact area is increased, reducing the rate towards the center of the wafer.

Figure 8 compares the removal rates for SiO_2 and SiO for templates of different pocket depths, all other conditions being identical. The slurry was diluted to 0.12 w/o silica to limit the maximum SiO rate to <100 nm/min. As described above, the rate increases with pocket depth until $(d - t) \sim 0$, as the polishing action moves from one regime to another. This increase is not linear with $(d - t)$, as variation in t of ±0.5 mil have no effect on the rate. The large difference in rates between Cases 3a and 3b may occur because of a change in the load distribution between the wafer and the template.

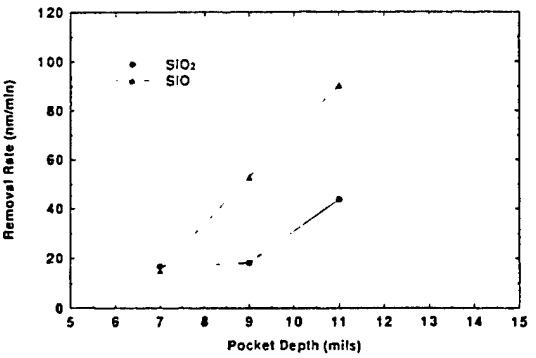

Fig. 8. Removal rates of SiO_2 and SiO for different pocket depths (t = 11 mils, F = 360 N, IC-1000 pad, ILD-1300 slurry with 0.16 w/o silica).

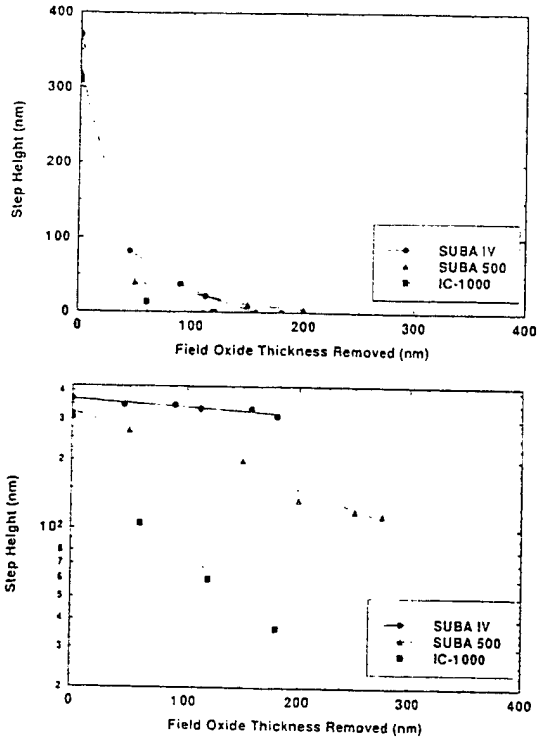

Fig. 9. Step height of (a, top) 25 and (b, bottom) 200 μm wide lines on SUBA-500, and IC-1000 pads as a function of field oxide thickness removed (t = 11mils, d = 9 mils, F = 360 N, v = 0.83 m/s, SC-1 slurry).

Planarization Using CMP

The main object for using CMP for ILD applications is for both local and global planarization. We planarized isolated lines and arrays of varying widths on 11 mil thick wafers with 9 and 11 mil template pocket depths. The polishing parameters were selected to be in the range where the removal rate is independent of applied load and velocity. Figures 9a and b show the step height of 25 and 200 μm wide isolated lines as a function of field oxide thickness removed for SUBA-IV, SUBA-500, and IC-1000 pads. Here the pocket depth is 9 mils. The 25 μm wide line is planarized on all the three pads, when a maximum of 200 nm of field oxide is removed. The 200 μm wide feature, however, is planarized only on the hard IC-1000 pad, as the softer pads tend to conform to the surface topography over such long distances. The data are fitted to an equation of the form $s = s_o \exp(-cD)$, where s_o is the initial step height, D is the field oxide thickness removed, reducing the feature height to s, and c is a constant related to the pad deformation length.[12] The value of c for the SUBA-IV, SUBA-500, and IC-1000 pads is found to be in the ratio 1:3:12 and roughly follows the compressibilities of the pads. As expected, the harder pad planarizes larger features at a faster rate than the softer pads.

A comparison of the planarization of a 200 μm wide line is made in Fig. 10 for SC-1 and ILD-1300 slurries. In both cases, the pocket depth is 9 mils, and the slurry concentrations are adjusted to give a field oxide removal rate of 50 nm/min. The ILD-1300 slurry reduces the step height of this line at a faster rate than SC-1 slurry. In the same plot, the step height of a 200 μm wide feature is plotted when the wafer was placed in template with a pocket depth of 11 mils. The planarization of this feature proceeds at an even faster rate.

The end point is reached when the oxide is completely removed from the tops of the counterelectrodes. The total polishing time is calculated knowing the field oxide thickness and the oxide removal rate. Because of the high run-to-run reproducibility in removal rate, we are able to complete the polishing process in a single attempt. The uniformity in the field oxide thickness across the wafer after CMP is ±10 nm, and no *in situ* end-point detection scheme is required.

Discussion

In the direct contact mode, our results are in agreement with earlier reports and with the mechanical models developed so far. Preston's equation is followed and the removal rate is not strongly influenced by the chemical reactivity of the oxide (the removal rates of SiO_2 and SiO being comparable). As the pad-wafer contact area is increased with increasing load, the slurry does not reach the oxide surface and the removal mechanism is mainly mechanical. This results in poor selectivity between different materials, decrease in rate with pad usage, and nonuniformities in oxide thicknesses across the wafer. The absence of polishing in the wafer gliding mode can be explained based on the same models, as in this regime, the load is applied entirely to the rim of the template, and there is no direct pad-wafer contact. As the slurry particles are not pressed against the wafer surface, both the chemical reaction rate and the mechanical removal of the reacted species is affected.

In the semidirect contact mode, the behavior is not predicted by any of the models. In these models, the mechanical and chemical processes in CMP are treated separately, whereas in reality both processes occur simultaneously. In this intermediate regime, the surface area undergoing a chemical reaction is increased by increasing the pocket depth and relative velocity. The oxide removal rate first increases as the pad-wafer contact is decreased, allowing more surface area to participate in the chemical reaction. The limited pad-wafer contact is sufficient to remove the reacted species. With further decrease in pad-wafer contact area (or increase in h), the rate begins to decrease as the mechanical activity of the pad is reduced. The removal rate in this mode is dependent on the chemical reactivity of the oxide, a weaker oxide producing a larger surface concentration of weakly bonded hydroxylated molecules. The planarization of protruding features is carried very efficiently with a hard pad. The pattern sensitivity and the dependence on the mechanical properties of the pad are in agreement with previous report.[12-14]

Conclusion

It is beyond the scope of this work to answer all the questions concerning CMP. However, the data presented here show the importance of the fluid layer in designing CMP equipment and in establishing a planarization process. The experimental results presented in this report on 2 in. diam wafers, clearly demonstrate that by increasing the wafer-fluid contact area and improving the slurry flow across the wafer, the oxide removal rate can be made independent of the polishing parameters over a wide range. This CMP pro-

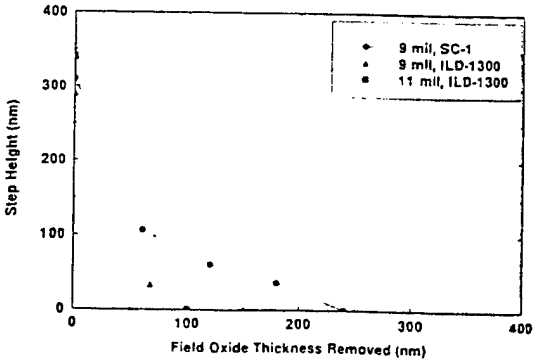

Fig. 10. Step height of 200 μm wide lines as a function of field oxide thickness removed (F = 360 N, v = 0.83 m/s, IC-1000 pad).

cess has a high run-to-run reproducibility, eliminating the need of expensive equipment for pad surface conditioning and end-point determination. As the removal rate is mainly dependent on the chemical properties of the oxide, high selectivity between different dielectrics and metals can be obtained by the selection of suitable slurries. Another advantage of the process is that high planarization rates are achieved at relatively low slurry concentrations. This combined with increased pad life reduces the cost of consumables, a major consideration in IC manufacturing. A more detailed modeling of the process is needed to further improve the understanding of various factors involved in polishing and their interactions.

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Self-shunted $Nb/AlO_x/Nb$ Josephson junctions

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Abstract—**We describe the fabrication and properties of high critical current density (J_c) $Nb/AlO_x/Nb$ Josephson junctions with deep-submicron dimensions. The junctions are fabricated using a planarized process in which all levels are patterned using a combination of optical and electron beam lithography. The base and counter electrodes are defined by reactive ion etching using quartz etch masks to give a minimum feature size of 0.2 microns. For J_c = 2.1 mA/μm² and junction area less than 0.1 μm² the devices are self-shunted and exhibit nonhysteretic *I-V* characteristics. A small hysteresis in the larger junctions is caused by heating in the electrodes.**

I. Introduction

Most of the applications of the Josephson effect in superconducting electronics such as SQUID based magnetic sensors, Josephson integrated circuits (ICs) (e.g., digital devices based on rapid single-flux-quantum (RSFQ) logic [1]), array oscillators [2],[3], and voltage standards [4] require Josephson junctions with nonhysteretic *I-V* characteristics. In present day $Nb/AlO_x/Nb$ technology, the intrinsically hysteretic (underdamped) tunnel junctions are shunted by normal metal resistors (so called resistively shunted junctions, RSJ) to achieve overdamped junctions. From a fabrication point of view, making RSJ has certain drawbacks as it involves additional processing for the resistors, via holes, and wiring. This increases the effective area of the junctions and restricts the level of integration in circuits. For certain high-frequency applications the parasitic inductance of the shunt resistor can cause degradation in performance [3]. The use of intrinsically overdamped or self-shunted junctions would then be desirable for IC applications.

Recently overdamped junctions made from double barriers of the type $Nb/AlO_x/Al/AlO_x/Nb$ were reported [5],[6]. These devices show good Josephson behavior and have larger characteristic voltages $V_c = I_cR_N$ than superconductor-normal metal-superconductor (SNS) type junctions [7] . Here I_c is the critical current and R_N is the normal state resistance of the junction. However, the V_c values obtained (~ 0.24 mV) were still much smaller than the intrinsic value for $Nb/AlO_x/Nb$ junctions (~ 2 mV), which would severely limit the high-frequency performance of the junctions since the response time in the overdamped regime scales inversely as V_c. Also, because of the double barrier, these devices have an inherently low critical current density J_c.

The J_c of Josephson junctions imposes a restriction on the maximum integration level in ICs , since the I_c of the junctions is usually fixed by design considerations. Therefore, increasing J_c would allow reduction of device size. The maximum speed of devices based on RSFQ logic scales roughly as square-root of J_c [1] and hence, for a fixed I_c, as inverse square-root of device area. Also the white noise limited sensitivity of a SQUID [8] improves with increasing J_c, so does the maximum power generated in array oscillators. The issue of nonhysteretic *I-V* characteristics is also directly related to J_c. Indeed, the McCumber parameter $\beta_c = 2\pi(I_cR_N)^2C_s/(\Phi_0J_c)$ characterizing the hysteresis decreases with increasing J_c so far as the I_cR_N product remains unaffected. Here C_s is the specific capacitance of the junction and Φ_0 is the flux quantum. Thus junctions with high enough J_c can be intrinsically overdamped ($\beta_c < 1$) and would offer significant improvement in device performance. Nb trilayer based Josephson junctions with J_c as high as 4 mA/μm² [9] and with deep-submicron dimensions [10] have been demonstrated. But even at $J_c > 3$ mA/μm², these devices showed some residual hysteresis. Two possible reasons for this are heating in the electrodes due to the high currents involved and parasitic capacitance contributing to increase in β_c.

II. Fabrication

In order to increase the flexibility of our implementation [11] of the PARTS process [12] for deep-submicron circuits, we have further developed the process to permit patterning by both electron beam lithography (EBL) and photolithography in all layers. This allows us, for example, to reduce the area of the base electrode (BE) and thus the BE – wiring layer overlap which is the

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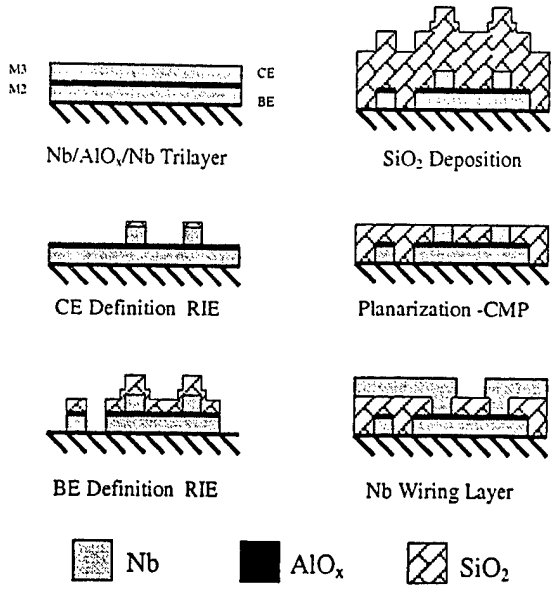

Fig. 1. Process flow for the fabrication of deep-submicron junctions using EBL patterned quartz etch masks and chemical mechanical polishing.

primary cause of parasitic capacitance. In addition to the present work, this EBL PARTS process has also enabled our group to make simple RSFQ circuits that operate to 750 GHz [13] as well as high-quality single electron transistors (SET). The SET results [14],[15], in particular, illustrate the capabilities of the process which has been used to fabricate Nb trilayer transistors having high quality junctions with areas down to 0.01 μm^2. These transistors have modulation amplitudes of up to 60 μV and a noise performance comparable to the standard Al junction transistors.

The fabrication process flow is shown in Fig.1. A Nb/AlO$_x$/Nb trilayer is deposited on a 50 mm diameter oxidized Si wafer in a cryopumped system with both Nb and Al films DC magnetron sputtered. The base electrode (BE) and counter electrode (CE) are 150 nm thick and the Al interlayer is ~ 8 nm thick. The J_c is controlled by the O_2 exposure (pressure×time) during oxidation of the Al interlayer. For the range of high J_c explored (60 $\mu A/\mu m^2$ - 2.5 $mA/\mu m^2$) in our experiments, the dependence of J_c on O_2 exposure is in good agreement with [9]. Accordingly, oxidation at 1.0 mTorr of O_2 for 10 min. gave a J_c of 2.1 $mA/\mu m^2$. PMMA / P(MMA/MAA) bilayers were used as both EBL resist and DUV resist for contact printing for all layers. A 50 nm thick layer of RF-sputtered SiO_2 (quartz) is lifted off to form an etch mask for the CE. The junction is then defined by a reactive ion etch (RIE) of the Nb CE in SF_6 plasma. Although the Al interlayer acts as a natural

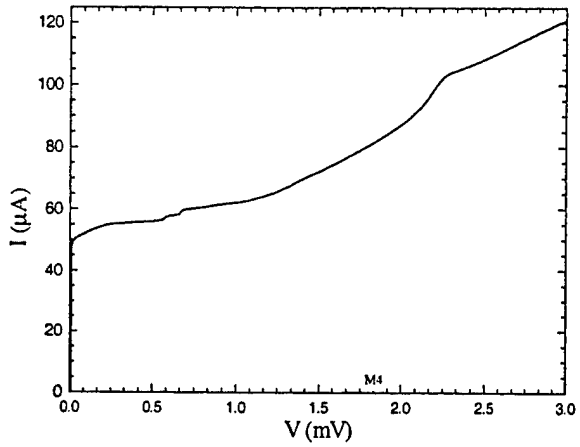

Fig. 2. The *I-V* characteristics of a 0.2 μm × 0.2 μm junction at $T = 4.2$ K.

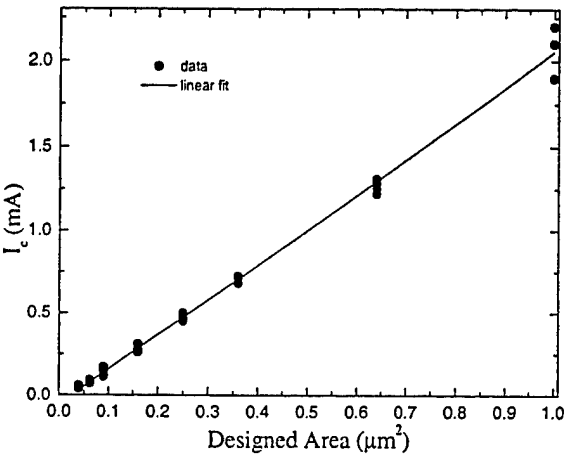

Fig. 3. Critical current scaling for 41 junctions on the same 0.7 mm square chip at $T = 4.2$ K.

etch stop, the precise termination of the etch is critical for obtaining deep-submicron features and is achieved by using an optical end point detector based on measurement of the intensity of certain fluorine lines. A 120 nm quartz etch mask is then lifted off for the BE, which gets defined by a wet etch of the Al interlayer followed by another RIE of the Nb base layer. 550 nm of quartz is then deposited to form the dielectric layer which is planarized using a chemical-mechanical polish (CMP) step [16]. The residual 5-10 nm of quartz remaining after planarization on top of the CE is removed using a CHF_3 + O_2 oxide etch which exposes the top of the junctions. Finally a 200 nm thick Nb wiring layer is lifted off. If required, resistor levels and a contact via level can be added before the wiring layer.

III. Device Characteristics

The results are presented for a J_c = 2.1 mA/μm^2 wafer. The designed junction area ranged from 0.02 μm^2 to 4 μm^2. More than 50 SQUIDs and 200 single junctions have been measured. The yield was greater than 95% for devices 0.04 μm^2 and larger. The *I-V* characteristic of a single junction of 0.04 μm^2 designed area is shown in Fig. 2. The scaling of I_c with designed area for some 40 junctions on one chip at 4.2 K is shown in Fig. 3. The total spread of I_c at 4.2 K across the wafer was less than 20% for all areas. R_N was measured at low voltages just below the critical temperature T_c of the electrodes. The measured I_cR_N product was 2.0 mV with less than 20% spread for all areas. C_s was estimated as ~ 90 fF/μm^2 from *LC* resonance in SQUIDs fabricated on the same wafer. The uncertainty in this estimate is no better than 40%, due to the finite width of the resonance steps and uncertainty in the SQUID inductance. The main contribution to the parasitic capacitance (C_p) of the devices is the overlap capacitance between the BE and wiring layer. The ratio C_j/C_p , where C_j is the junction capacitance, is the smallest for the smallest device area since the overlap area is set by fabrication constraints. For 0.04 μm^2 junctions the BE was 0.8 μm wide and the overlap area was 0.6 μm^2. Using a simple parallel plate formula with quartz as the dielectric, gives C_p = 0.16 fF and C_j/C_p = 22. Neglecting parasitic capacitance, we get β_c = 0.6.

All devices smaller than 0.1 μm^2 were found to be self-shunted at 4.2 K and showed no measurable hysteresis. However, larger devices showed a noticeable hysteresis which increased with device area (or I_c). The quantity $(I_c-I_r)/I_c$ which serves as a measure of the hysteresis, increases from 2% for 0.25 μm^2 junctions to 22% for 1 μm^2 junctions. Here I_r is the retrapping current. On lowering the temperature, this hysteresis becomes smaller (at 1.8 K , it is 14% for 1 μm^2 junctions), which indicates heating in the electrodes as the likely cause of hysteresis.

The quasiparticle *I-V* characteristic for a 0.5 μm×0.5 μm and 1.0 μm×1.0 μm junctions at 1.8 K are shown in Fig. 4a. A small magnetic field is applied parallel to the plane of the junctions to suppress the Josephson current. The ratio of the subgap resistance to the normal state resistance R_j/R_N is ~ 1. It is known that transport in the subgap region of high J_c junctions is dominated by processes involving multiple Andreev reflections (MAR) [17]. Since at these high J_c's the oxide barrier is only one or two monolayers thick on average, there exists a large number of atomic scale shorts beween the superconducting electrodes. As the dimensions of these shorts are much smaller than the coherence length ξ (~

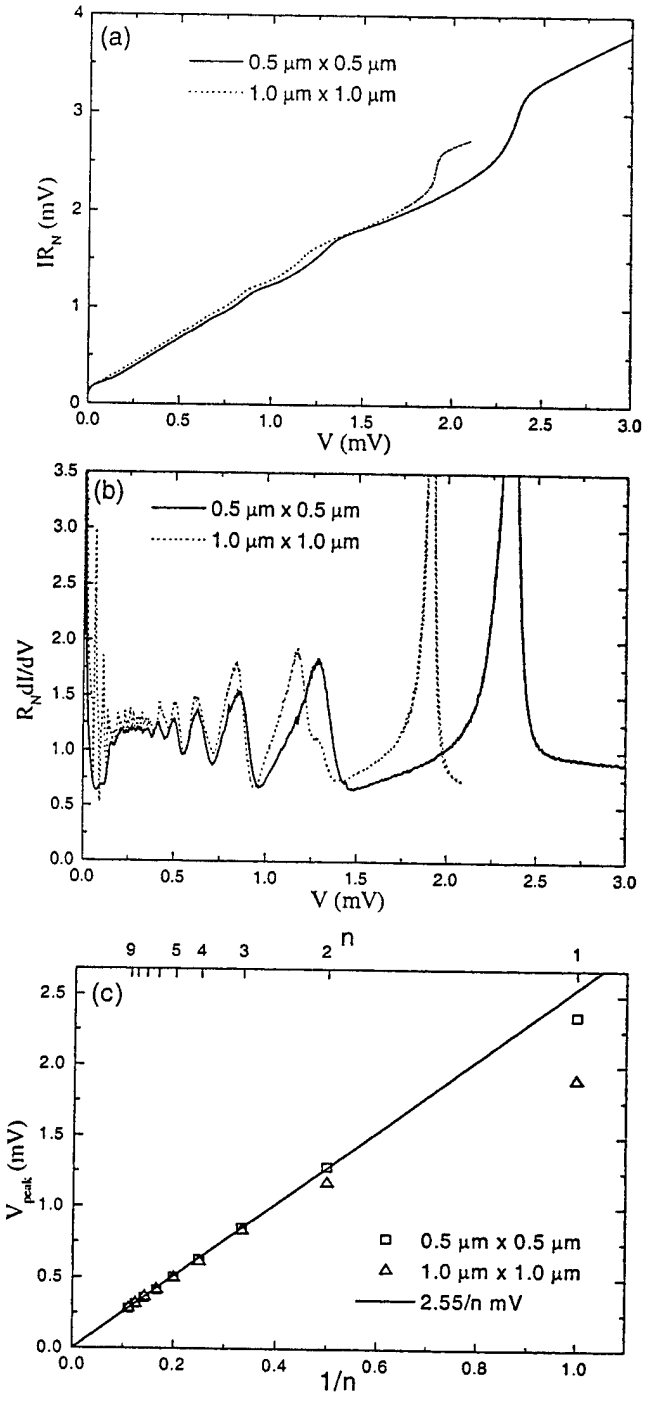

Fig. 4. (a) The quasiparticle *I-V* characteristics of a 0.25 μm^2 (solid line) and 1.0 μm^2 (dashed line) junctions at T = 1.8 K; (b) the dynamic conductances of the same junctions at T = 1.8 K; (c) the locations of the MAR peaks as a function of the reflection order n. The solid line represents the predicted dependence 2Δ/n for 2Δ = 2.55 mV.

38 nm for Nb) and the electron mean free path in the electrodes, each of these "microshorts" or "pinholes" acts as a single ballistic channel for quasiparticle transport [18]. MAR, the mechanism responsible for transport in these microshorts, manifests themselves as peaks in the dynamic conductance at voltages equal to $2\Delta/n$, where Δ is the temperature dependent superconducting gap in the electrodes and n is an integer. The dynamic conductance ($G_D = dI/dV$) showing the MAR peaks for the two devices is plotted in Fig. 4b. The positions of these MAR peaks are plotted in Fig. 4c. The effect of heating in the electrodes is clearly seen as suppression of Δ at higher voltages. The zero voltage singularity in the dynamic conductance follows a power law $G_D(V) \propto 1/V^{\alpha}$, with the exponent α ranging from 0.6 to 0.8, which differs somewhat from the theoretically predicted value of 0.5 [19]. This deviation and spread in the measured value of α could be due to the Josephson current not being completely suppressed. A detailed analysis will be presented elsewhere.

IV. Applications

Fig. 5 shows the *I-V* characteristic of a dc SQUID fabricated on the same wafer. Flux is coupled into the SQUID loop by passing a current trough a modulation coil surrounding the SQUID loop. A current of 1.65 mA in the modulation coil injects one flux quantum Φ_0 in the SQUID loop. The inset in Fig. 5 shows the voltage modulation of the SQUID at a bias current I_B of 276 μA. The maximum voltage-to-flux transfer is ~1 mV/Φ_0. The noise performance of these devices will be presented elsewhere.

Achieving higher operating speeds through better device integration for digital RSFQ circuits was one of the principle motivations for developing high J_c self-shunted junctions. For technology evaluation, superconducting frequency dividers based on the RSFQ T-Flip Flop were designed and fabricated using self-shunted Josephson junctions [13]. These devices, consisted of 8 junctions with a minimum dimension less than 0.1 μm^2. The operating speed in these TFFs is indicated by the maximum frequency for which accurate frequency division is possible, f_{max}. A f_{max} of 770 GHz was achieved at 4.2 K for a J_c of 2.5 mA/μm^2.

As noted, the parasitic inductance of shunt resistors limits the high frequency and high power performance of Josephson effect array oscillators. The nonhysteretic junctions described here have been tested for oscillator applications by studying phase-locking between two 0.25 μm × 20 μm junctions having critical currents of about 10 mA. These two junction cells show good high-frequency locking up to the superconducting gap voltage [20] and so appear promising for oscillator applications.

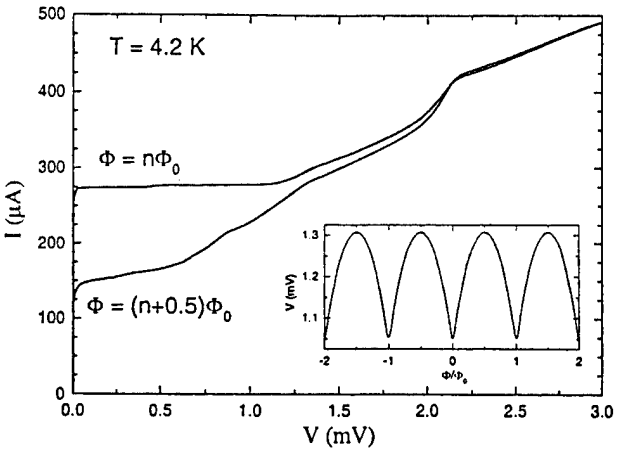

Fig. 5. The *I-V* curve of a dc SQUID with 0.25 μm × 0.25 μm junctions and loop inductance ~ 5 pH. The inset shows the voltage modulation at a bias current of 276 μA.

V. Conclusions

We have fabricated and characterized intrinsically overdamped Josephson junctions using Nb/AlO_x/Nb trilayers with J_c = 2.1 mA/μm^2. Deep-submicron junctions with a small parasitic capacitance due to the overlap between BE and wiring layer are achieved by using a fabrication process in which all levels are patterned by EBL. The junctions with dimensions smaller than 0.1 μm^2 show nonhysteretic *I-V* characteristics while junctions with larger dimensions have a small hysteresis due to heating in the electrodes.

Acknowledgments

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Appendix C

Off-chip Detection of Radiation from a Linear Array Oscillator with a Spiral Antenna

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Abstract—**Radiation from a linear array oscillator with a spiral antenna has been measured using an off-chip coupled bolometer. The array oscillator has a distributed array structure with 300 resistively shunted junctions which are placed in the groups of 6 junctions. The array oscillator was fabricated on a Si wafer with a two-arm spiral antenna. The chip was attached to a Si lens with an anti-reflection coating. Rather large power (> 100 nW) was detected at a number of array bias voltages V_{bias} from 115 mV to 196mV, which correspond from 185 GHz to 315GHz. The maximum measured power was 550 nW at V_{bias}=125 mV (200GHz).**

I. Introduction

Compact millimeter and submillimeter wave sources are desired in fields such as radio astronomy and molecular photo-spectroscopy. Superconducting oscillators have generated enough power to operate on-chip SIS mixers in the submillimeter wave region [1]. However, in order to use superconducting oscillators for off-chip applications such as molecular spectroscopy, it is necessary to couple the radiation to free space. Several methods have been demonstrated to couple radiation from superconducting oscillators to free space using a quasioptical junction array [2], a 2D array with a finline antenna [3], a 2D array with high Tc junctions [4], and a Flux-flow oscillator with a tapered slotline antenna [5]. 1D series array superconducting oscillators are particularly suitable for off-chip applications because they have large available power and large source impedance [6]. However, there has been no report of coupling the radiation from 1D array oscillators to free space.

In this paper, we report the first results of coupling radiation from a 1D array oscillator to free space. A Si lens with an anti-reflection coating and an on-chip spiral antenna are used to couple the radiation from the oscillator to free space. The radiation power is measured with an off-chip coupled Si composite bolometer [5].

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II. Structure

Fig. 1 shows a schematic view of a fabricated 1D series array oscillator with a spiral antenna. The antenna is a planar two-arm logarithmic spiral antenna. The shape for a single arm of a planar spiral antenna is represented by the following function [7]

$$\frac{r}{\lambda} = \exp\{c(\theta - \theta_0)\} \qquad (1)$$

with (r, θ) polar coordinates, λ wave length, c a dimensionless constant and θ_0 the initial angle. In order to make a close connection between the feeding point of the antenna and the array oscillator with a large area, we

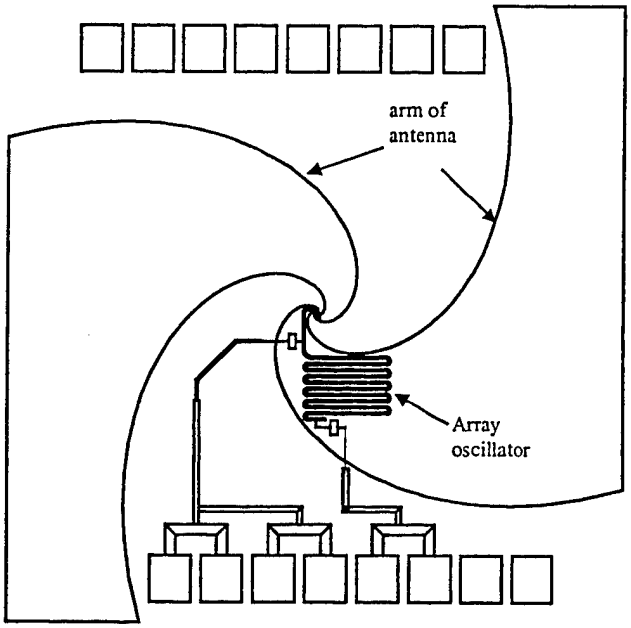

Fig. 1. Schematic top view of an array oscillator with a spiral antenna (chip size 6×6 mm^2).

chose wider arms for the antenna (c=1.0) than those used for SIS mixers [7]. Mounting a two arm spiral antenna on to a half-space of dielectric (approximated by a lens) gives an antenna impedance

$$Z_{ant} = \frac{60\pi}{\sqrt{(1+\varepsilon_r)/2}} \approx 75\Omega \qquad (2)$$

where ε_r=11.7 is the dielectric constant of Si. Because the length of the arm is more than 3 mm, the impedance should be constant in the frequency range of interest (> 100 GHz) [7].

The power from an array oscillator matched to the load is given by $P \approx R_L I_c^2/8$, where R_L is the load impedance and I_c is the critical current of the junctions [6]. Increasing the source power, therefore, requires increasing I_c while keeping $\beta_L < 1.0$ and $\beta_c < 1.0$ to avoid unstable dynamics of the array. In recent array oscillators with large power (> 100 μW), a large number of junctions ($N \sim 2000$) with a large area (~ 1.5×84 μm^2) and a large critical current density ($J_c \sim 10$ kA/cm^2) were used [8]. As the first trial, however, we chose a modest junction size (2×18 μm^2), $J_c \approx 5$ kA/cm^2, and N (= 300) to obtain good process yields. The oscillator is a distributed array with resistively shunted $Nb/AlO_x/Nb$ junctions which are placed in 6 junction groups. Adjacent junctions in the group are separated by 12μm. Each group is spaced by half or one wavelength (λ_0) at the designed primary operating frequency of 400GHz. The junctions are serially connected on a 20 μm width microstrip line. One arm of the antenna is used as the ground plane of the array oscillator. The other arm of the antenna is connected to one end of the microstrip line. The other end of the microstrip line is terminated by a quarter wavelength ($\lambda_0/4$) stub. The designed characteristic impedance of the microstrip line is $Z_0 = 6.2\ \Omega$. A detector junction to measure the rf currents is placed between the antenna and the array oscillator. The distance from the detector junction to the first group of the array is λ_0. and that to the feeding point of the antenna is 1.5 λ_0. The size of the detector junction is the same as that of the array junctions. The capacitance of the junctions is estimated from the specific capacitance of 61 $fF/\mu m^2$ to be 2.2 pF. The parasitic inductance L associated with the external shunt resistor is estimated to be 0.15 pH. The shunt resistance R_j is designed to be Z_{ant}/N (~0.25Ω).

Fig. 2 shows a cross section of a junction in the array oscillator. The fabrication process is described in detail in reference [9]. The outline is as follows. A 2-inch Si wafer was patterned with a bilayer PMMA mask which has a large undercut required to lift-off sputtered Nb(120nm)/AlOx/ Nb(60nm) trilayer films which form the junctions and the microstrip line. The junction area was defined by reactive ion etching (RIE) using a PMMA mask patterned with electron beam lithography (EBL). A 120nm-thick SiO film for junction isolation and a 80nm-thick PdAu film used as the shunt resistor, with 1.5nm-thick Ti as an adhesion layer, were deposited using the same PMMA mask. After lift-off, Nb counter electrodes on contact windows were removed by RIE. A 400nm-thick Nb wiring was patterned by lift-off using a bilayer PMMA mask. The extra PdAu film around the Nb wiring layer was removed with a wet etch in a KI solution using the Nb wiring as the mask.

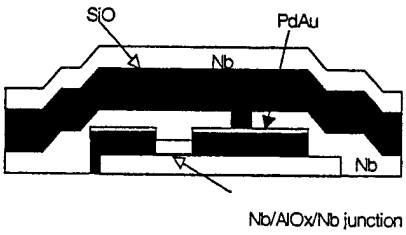

Fig. 2. Schematic of a cross section of a junction in the array oscillator

The shunt resistors were defined by etching the Nb wiring. 800nm of SiO, as the dielectric between the Nb microstrip line and the ground plane (one arm of the spiral antenna), was deposited after patterning with the bilayer mask. After removing the SiO film on the contact window by lift-off, the spiral antenna was formed by depositing a 400nm-thick Nb film.

III. Experimental

The measurement of current-voltage curves and radiation characteristics of a fabricated chip were made in a vacuum dewer schematically shown in Fig. 3. An array chip was attached on the flat surface of a Si extended hemispherical lens with grease (APIEZON L). The lens has a 12 mm diameter, 1.5 mm extension, and 94 μm Stycast anti-reflection coating. The lens was held with a copper ring, which was attached to a copper heat sink on the 4.2K stage in the dewer. A silicon composite bolometer was mounted on an end of a Winston cone, through which radiation from the oscillator chip was

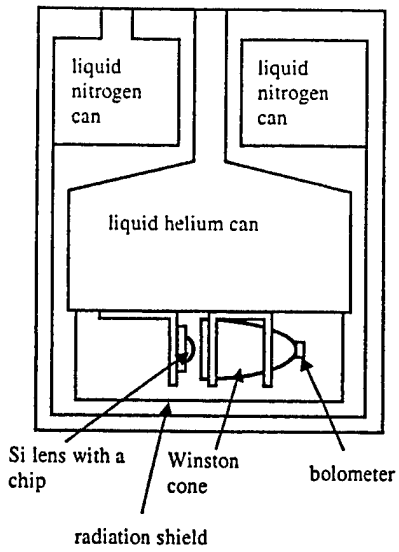

Fig.3. Schematic view of an experimental setup for off-chip detection of radiation power

collected. The diameter of the open end of the cone was 2.5 cm and the length of the cone was 6 cm. The separation of the open end of the cone and the chip was 5 mm. The oscillator and the bolometer mount were enclosed in a copper box to shield them from thermal radiation. The bias current to the array was chopped at 10 Hz between the zero voltage state and the bias voltage under test. The minimum measurable power was limited to about 10 nW by external noise. The calibration of the bolometer was made using a far-infrared laser (wave length = 393 μm).

IV. Results and Discussion

The radiation power from a fabricated array oscillator was measured. The average critical current of the junctions in the array was 1.5mA and the average junction resistance was 0.3Ω. The detected power of radiation from the array is shown in Fig. 4 as a function of the dc bias voltage on the array and the corresponding frequency calculated using the Josephson equation. The frequency characteristics of the detected power are rather complicated. Rapid changes of the power in a small voltage range (~ 0.6 mV) may be caused by a cavity resonance of the Winstone cone. More than 100 nW of power was measured at a number of bias voltages between V_{bias}=115 mV and V_{bias}=196 mV. The maximum detected power (~550nW) was obtained at V_{bias}=125 mV. However we could not detect the radiation power above V_{bias}=200mV. Heating caused by bias currents flowing through the shunt resistor may suppress the generation of rf power at higher bias voltages.

Clear Shapiro steps were observed in the current-voltage curves of the detector junction at many of the data points. Fig. 5 shows a current-voltage curve of the detector junction when the array was biased at 165 mV. The rf current I_{rf} through the detector junction can be estimated from the size of the Shapiro step using an RLCSJ model [6]. The power P_{ant} fed to the antenna can be calcurated by the following equation

$$P_{ant} = I_{rf}^{\,2}[\mathrm{Re}\{Z_L'\}]/2 \qquad (3)$$

where Z_L' is the load impedance seen from the detector junction. Z_L' can be represented with Z_{ant} and Z_0 as follows

$$Z_L' = \frac{Z_0(Z_{ant}\cos\beta l + jZ_0\sin\beta l)}{Z_0\cos\beta l + jZ_{ant}\sin\beta l} \qquad (4)$$

where l is the distance between the detector junction and the feed point of the antenna, and β is the phase constant. Fig.6 shows Re{ Z_L'} and P_{ant} calculated from the Shapiro steps of the detector junction as a function of frequencies. From a comparison of Fig. 4 with Fig. 6, about 10% of the power fed to the antenna was coupled

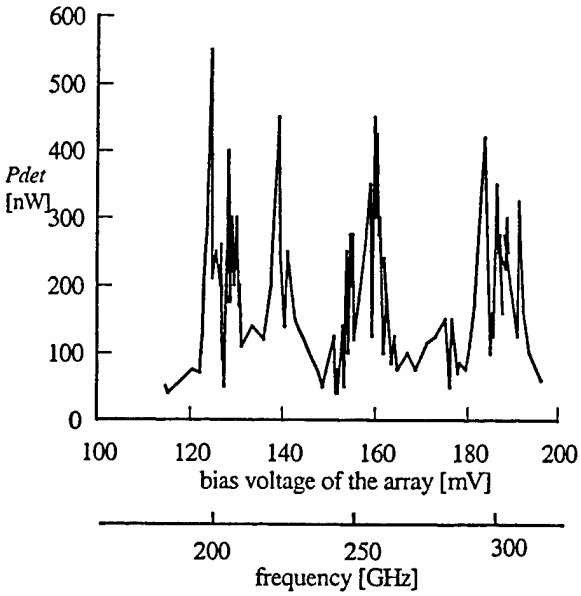

Fig. 4. Detected power P_{det} of radiation from an array oscillator with a spiral antenna.

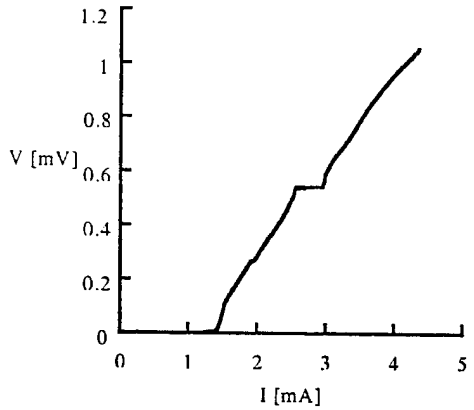

Fig. 5. I-V curve of the detector junction with array biased at 165mV

to the bolometer. However, the measured power is enough to pump an off-chip coupled SIS mixer operated at 200~300 GHz.

Recent advances in fabrication technologies and design enable us to make array oscillators having an available power approaching a milliwatt in the submillimeter wave region. We have designed, fabricated, and tested such arrayswithout antennas. The arrays were fabricated using the fabrication technologies mentioned above. The fabricated array has large area junctions ($2 \times 80\ \mu m^2$) in order to increase the critical current. The tested array with N=498, I_c=10mA, and R_j=55mΩ delivered 0.4mW of power to a load of 8Ω at 410GHz as measured by an on-chip detector junction operated in the video mode to avoid heating. Several mW of source power for a 50Ω load can be expected by using an array with N=3000. Therefore, we can expect

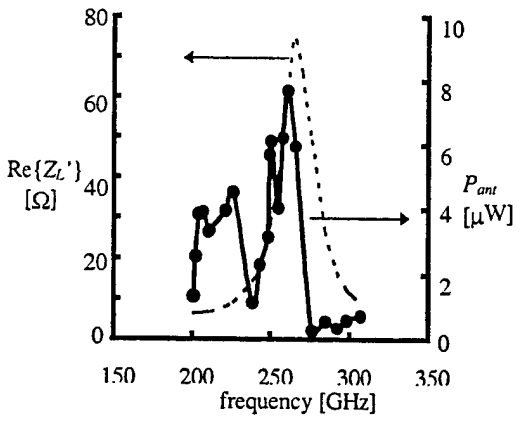

Fig. 6. Real part of the load impedance Re{Z_L'}seen from the detector junction and estimated power P_{ant} fed to the antenna.

to couple several hundreds μW of radiation power to free space by connecting such array oscillators with an antenna as described above.

IV. Summary

In this paper, we describe off-chip measurement of radiation from an array oscillator with a spiral antenna. Rather large power (> 100 nW) was detected by an off-chip coupled bolometer at a number of bias voltages between 115 mV and 196 mV, which correspond to frequencies from 200 GHz and 315 GHz. The maximum power (550 nW) was obtained at the bias voltage 125 mV (200 GHz). Our results demonstrate the feasibility of using an antenna to couple mm and submm wave from high power array oscillators for off-chip applications.

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